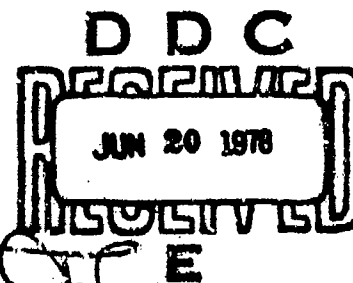FOR FURTHER TRAN ~~II~~

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RADC-TR-78-92
Final Technical Report
April 1978

BROADBAND MODEM II

Bruce E. Gillingham
Robert C. Davis

Harris Corporation

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Air Force Systems Command
Griffiss Air Force Base, New York 13441

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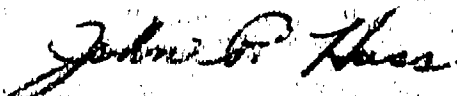
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The objective of this program was to optimize the techniques developed on the previous contract (Contract F30602-74-C-0263) from a cost and performance point of view and to implement an experimental modem suitable for extended test at RADC providing bandwidth efficient signalling for the line-of-sight microwave system. Specifically, spectral efficiency compliant with FCC Docket 19311 was required. A bit error rate of 5×10^{-9} at an E_b/N_o of 22 dB for two bits/hertz of RF bandwidth operation or at an E_b/N_o of 16 dB for one bit/hertz of RF bandwidth operation was desired. (Cont'd)

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20 (Cont'd)

An experimental modem was constructed and successfully tested, both in the laboratory and at RADC. All design requirements were met. Most notably, the performance goal of emission requirements as described in FCC Docket 19311 was met. The acquisition performance objective of 20 ms for a frequency offset of 20 kHz was met, as was the performance objective of 5×10^{-9} bit error rate at an E_b/N_0 of 16 dB for one bit/hertz operation. The design objective of a 5×10^{-9} bit error rate at an E_b/N_0 of 22 dB for two bits/hertz operation was exceeded in back-to-back tests and was within 0.6 dB for a group-delay compensated LC8D radio.

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EVALUATION

The attainment of bandwidth efficient digital communications over line-of-sight (LOS) has been limited by non-linear power amplifiers. The optimum signal structures for bandwidth efficiency are those wherein the information is stored in the signal amplitude, i.e., amplitude shift keying (ASK). In order to perform well, ASK-type signal structures require linear operation. This forces one to attempt to linearize the amplifier (usually a traveling wave tube) by backing it off; however, this results in lower power outputs and thus lower system gain which can reduce system availability.

An alternative approach is to use techniques which store the information in phase or frequency (PSK or FSK) and are not effected by non linearities; however these signal structures are less bandwidth efficient than linearly derived structures. The emphasis in this program, and the study/breadboard effort which preceded it, was in optimizing the phase trajectory to minimize spectral occupancy but yet optimizing performance. The technique selected and implemented as optimum, was 4 level phase continuous FSK. It was determined during the course of the program that FCC 19311 could not be met exclusively with waveform design without compromising bit error rate (BER) performance. Consequently an rf waveguide filter was fabricated to reduce the spectral sidelobes to fit the FCC 19311 mask. The use of RF filters for spectral containment is an accepted technique; however, RF filtering cannot be used exclusively because of the excessive group delay and amplitude distortion introduced, necessitating the use of a complicated equalizer at the receiver. The best results are achieved by a combination of waveform design and RF filtering.

As a result of this combination of waveform design and RF filter design the experimental model developed on this program delivered 2 bits per Hz transmission and achieved a BER of 5×10^{-9} at an Eb/N_0 of 22.6dB. System gain is not compromised because amplifier non-linearities are not a factor. Performance is very competitive with presently reported linear or quasi-linear techniques which cannot provide as high a system gain because of the TWT backoff required to obtain linear operation.

BRIAN M. HENDRICKSON
Project Engineer

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SECTION 1.0

INTRODUCTION

1

1.0   INTRODUCTION

1.1   Objective

The objective of this program was to optimize the techniques developed on the previous contract (F30602-74-C-0263) from a cost and performance point of view, and to implement an experimental modem providing bandwidth efficient signalling for line-of-sight microwave systems. Specifically, spectral efficiency compliant with FCC Docket 19311 was required. A bit error rate of 5×10^{-9} at an E_b/N_0 of 22 dB for 2 bits/sec/Hz (B/Hz) of RF bandwidth operation or at an E_b/N_0 of 16 dB for 1 B/Hz of RF bandwidth operation was desired. These characteristics, provided in conjunction with hard-limiting radio sets, allow efficient conversion of analog FDM-FM line-of-sight microwave systems to digital operation by replacement of the modulation elements.

1.2   Approach

The program consisted of two main phases. During the first phase, an analytical study was undertaken to expand upon techniques developed on the previous program. It was desired that the experimental modem provide significantly improved performance over the previously constructed breadboard as well as additional operational features. In the second phase, the experimental modem was constructed and tested both in the laboratory and on an actual microwave radio.

1.3   Results

The experimental modem was successfully tested both in the laboratory and the Rome Air Development Center (RADC). All design requirements were met. Most notably, the performance goal of emission requirements as described in FCC Docket 19311 was met with some margin. The acquisition performance objective of 20 ms for an IF frequency offset of 20 kHz was met, as was the performance objective of 5×10^{-9} bit error rate at an E_b/N_0 of 16 dB for 1 B/Hz operation. The design objective of a 5×10^{-9} bit error rate at an E_b/N_0 of 22 dB for 2 B/Hz

operation was exceeded in back-to-back tests and was within 0.6 dB for a group-delay compensated LC8D radio.

A significant accomplishment of this program was developing an experimental modem which, unlike the previous breadboard, is simple to operate and stable in performance. All tests at RADC was performed with the modem as received from shipment without any realignment. Performance degradation from that obtained in the laboratory was negligible.

1.4   Report Organization

The results of the analytical effort are presented in Section 2.0. The design and construction of the modem are discussed in Section 3.0. In Section 4.0 the test program and results are presented. The conclusions are presented are in Section 5.0.

SECTION 2.0

ANALYTICAL RESULTS

2.0   ANALYTICAL RESULTS

2.1   Background

This section describes the analytical effort on this program.
On a prior contract (Contract F30602-74-C-0263) for Rome Air Development
Center (RADC), a study was performed to choose a bandwidth efficient
signalling scheme for the microwave line-of-sight channel. Design
objectives on the prior contract included 99 percent spectral occupancy of
one-half bit rate and 20 dB E_b/N_o for 10^{-7} error rate. Primarily
because of the microwave radio saturated TWT amplifiers, the signal design
effort on the prior contract was restricted to constant envelope signalling
schemes. This type signalling avoids problems caused by AM/PM conversion
characteristics of the TWT's.

The conclusion on the prior contract was that 4-ary continuous
phase FSK with frequency spacing equal to one-eighth the symbol rate
represented the best performance/complexity versus spectral occupancy
trade-off. On the prior effort, a unique technique was developed for
demodulating the 4-ary FSK signal such that near-optimum performance was
obtained. The technique was the subject of an "abstract of new technology"
on the prior contract.

After the prior study effort, a breadboard model of the modem
was constructed and the feasibility of the scheme was verified through both
laboratory measurements and actual microwave link tests at RADC. The
results are included in the final report (RADC-TR-76-117) to RADC.

As with most breadboard efforts, there were implementation
features of the modem that were operationally inconvenient, such as
acquisition of the phase detection reference loop. In addition several
difficult and critical timing adjustments were required to obtain predicted
performance. One of the primary motivations of the present contract was to
eliminate the difficulties and shortcomings associated with the original
breadboard. A stated design objective for the present effort was to
acquire 20 kHz frequency offset in 20 ms at an E_b/N_o corresponding to a
10^{-7} bit error rate.

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In the prior contract the spectral criterion imposed was 99 percent spectral occupancy in one-half bit rate RF bandwidth. For the present effort, the spectral criterion imposed is that of meeting the FCC Docket 19311 (See Appendix A) spectral mask for an authorized bandwidth of one-half bit rate. This criterion places a more stringent requirement on the side lobes of the transmitted spectrum than did the original 99 percent spectral occupancy criterion.

Another goal of the present study was to develop a technique for providing 1 B/Hz operation (again under FCC docket 19311 criterion) as well as 2 B/Hz operation.

New implementation techniques were to be investigated with an eye to reducing the cost and complexity of the original breadboard. Finally, an experimental modem was to be implemented incorporating the results of the study phase of the present effort. This modem was then to be used for tests at RADC on their microwave test facility.

2.2   Summary of Broadband Modem II Study Phase

This paragraph presents a brief summary of the major results and conclusions of the effort. A more detailed discussion follows in Paragraph 2.3.

2.2.1   FCC 19311 Compliance

Both 70 mHz IF Filter/Limiter and 8 GHz microwave waveguide filter approaches were investigated. The best IF filter/limiter combination provided theoretical E_b/N_o of 23.1 dB for a 5×10^{-9} bit error rate. The waveguide filter approach yielded theoretical E_b/N_o of 20 dB for a 5×10^{-9} bit error rate. The waveguide filter approach was adopted as the baseline. Discussions with waveguide filter manufacturers indicated that less than 1 dB of insertion loss could be achieved. Additionally, INVAR construction of the filter yielded tolerable detuning of less than ± 450 kHz over a 0° to 50° C temperature range. The waveguide filter selected is nominally 4-pole Butterworth with a 3 dB bandwidth of 16 MHz.

2.2.2   New Implementation Techniques

The "closed-loop reference derivation" technique was adopted for this modem. The basic idea is to use the known phase nodes of 4-ary FSK with which to compare the measured phase from the Quadrature Phase Detector (QPD) to determine the phase error to closest node. This error signal is filtered by a loop filter in the same manner as a normal PLL and the resultant signal used to drive the VCO which provides the QPD reference. This "closed-loop" reference derivation technique bears a close resemblance to COSTAS-type loops widely used to establish coherent references. This eliminated critical reference phasing problems in the original breadboard as well as simplified the modem reference generation. Sample and hold circuits were included in the phase detectors to alleviate the critical symbol timing problems encountered in the previous breadboard. The receiver IF filter was changed to 4-pole Butterworth with phase compensation, rather than the 4-pole Bessel used in the previous Breadboard.

2.2.3   Improved Acquisition

Computer simulations indicated a dual reference derivation loop bandwidth approach was required to acquire 80 kHz of frequency offset in 1 ms. A single loop bandwidth approach will acquire 20 kHz of offset in 20 ms or 80 kHz offset in 320 ms. The goal was modified in consultation with RADC to 20 ms acquisition with 20 kHz frequency offset. Therefore, a single loop bandwidth approach was adopted to simplify the hardware on the experimental modem.

2.2.4   Dual B/Hz Capability

A technique was developed to provide 1 B/Hz capability in addition to 2 B/Hz capability. Both capabilities are designed to operate in an authorized bandwidth of 14 MHz. Both modes meet corresponding FCC 19311 spectral masks using a common waveguide filter. The 1 B/Hz technique involves a relatively simple conversion technique at the demodulator IF input that exploits maximum equipment commonality between the two spectral capabilities.

2.3 Details of Study Phase

This section outlines the study effort undertaken to achieve the objectives of the Statement of Work for this program.

2.3.1 FCC Docket 19311 Spectrum Compliance

At the outset of this contract it was felt that one of the most challenging theoretical problems was to achieve compliance with FCC Docket 19311 spectral requirements. Figures 1 and 2 show the spectra for 1 B/Hz and 2 B/Hz modes for unfiltered 4-ary FSK relative to the appropriate spectral masks from FCC 19311. The 1 B/Hz mode uses frequency spacing of 1/4 symbol rate (mod-index 1/4) and the 2 B/Hz mode uses frequency spacing of 1/8 symbol rate (mod-index 1/8). As shown, the 1 B/Hz mode violates the mask as much as 15 dB and the 2 B/Hz mode violates the mask as much as 18 dB in the side lobes.

Two primary approaches for obtaining FCC 19311 compliance were pursued during the study phase. These were: (1) 70 MHz IF filtering followed by hard limiting at the modulator before interfacing with the 70 MHz IF radio input, and (2) 8 GHz microwave waveguide filtering. These approaches are described below.

2.3.1.1 IF Filter/Limiter Approach

The IF filter approach is shown in block diagram form in Figure 3. Originally, it appeared that the IF approach would be preferred over the waveguide filter approach from the standpoint of operational considerations. The IF filters could be readily changed or replaced to meet varying bit rate requirements in an operational system. It was decided that consideration of waveguide filtering should be deferred until an IF filtering approach could be thoroughly evaluated.

Consequently, an effort was undertaken to analytically characterize the IF filter approach. Important elements of this characterization were: (1) computation of radiated power spectrum, and (2) computation of modem performance (BER versus E_b/N_o). A FORTRAN computer program was written to perform these computations. The chief analytical tool used in

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Figure 2. 2 B/Hz Spectrum Without Filtering

Figure 1. 1 B/Hz Spectrum Without Filtering

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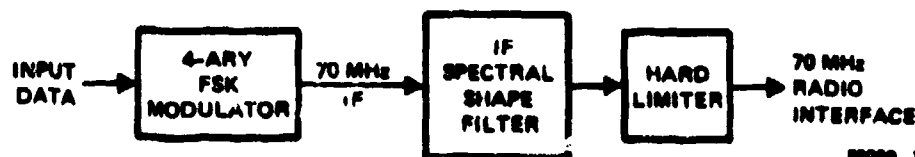
Figure 3. Basic IF Filter Approach to FCC Docket 19311 Compliance

this program is a Fast Fourier Transform (FFT) routine. Spectra are
obtained by averaging FFT's over many random symbol sequences. Time-domain
parameters necessary for computing modem performance are also computed with
the FFT. The time-domain quant'ties of most importance in determining
modem performance are phase measurements of the filtered (hence distorted)
received FSK waveform. The computer program also includes a portion which
computes the average symbol error rate given the distorted phase measure-
ments. The computer program is described in more detail and a listing is
presented in Appendix B. This program was used to produce the results
given below for both the IF and waveguide filter approaches to FCC 19311
compliance.

At the outset of the IF filter search a good analytical or intu-
itive grasp of the effects of the filter/limit combination was not avail-
able. The approach taken therefore was to try various combinations of what
seemed to be reasonable type filters and calculate spectra after the
limiter with the computer program. During this extensive iterative process
some intuitive understanding of necessary requirements on the filter for
meeting FCC 19311 began to emerge.

First and foremost among the characteristics of the filter/limit
combination is the limiter's restoration (to a large degree) of the prefilter
side lobe levels for many filters. Figure 4 is a case in point. The
spectrum is plotted versus $32 \left| f-f_c \right| T_s$ where f = frequency, f_c = center
frequency, and T_s is the 4-ary FSK symbol time. The quantity $\left| f-f_c \right| T_s$
is thus the number of symbol rates removed from center frequency. Here the
filter is an 8-pole 0.1 dB ripple Tchebycheff design with the 3 dB point
at 20 on the horizontal scale. The major offending side lobe prior to
filtering occurs at 32 on the horizontal scale and has level of -62 dB.
The Tchebycheff filter has an attenuation of 55 dB at this side lobe
frequency thereby placing the prelimiter side lobe level at -117 dB. As
shown, after limiting, the side lobe is restored to the -69 dB level for a

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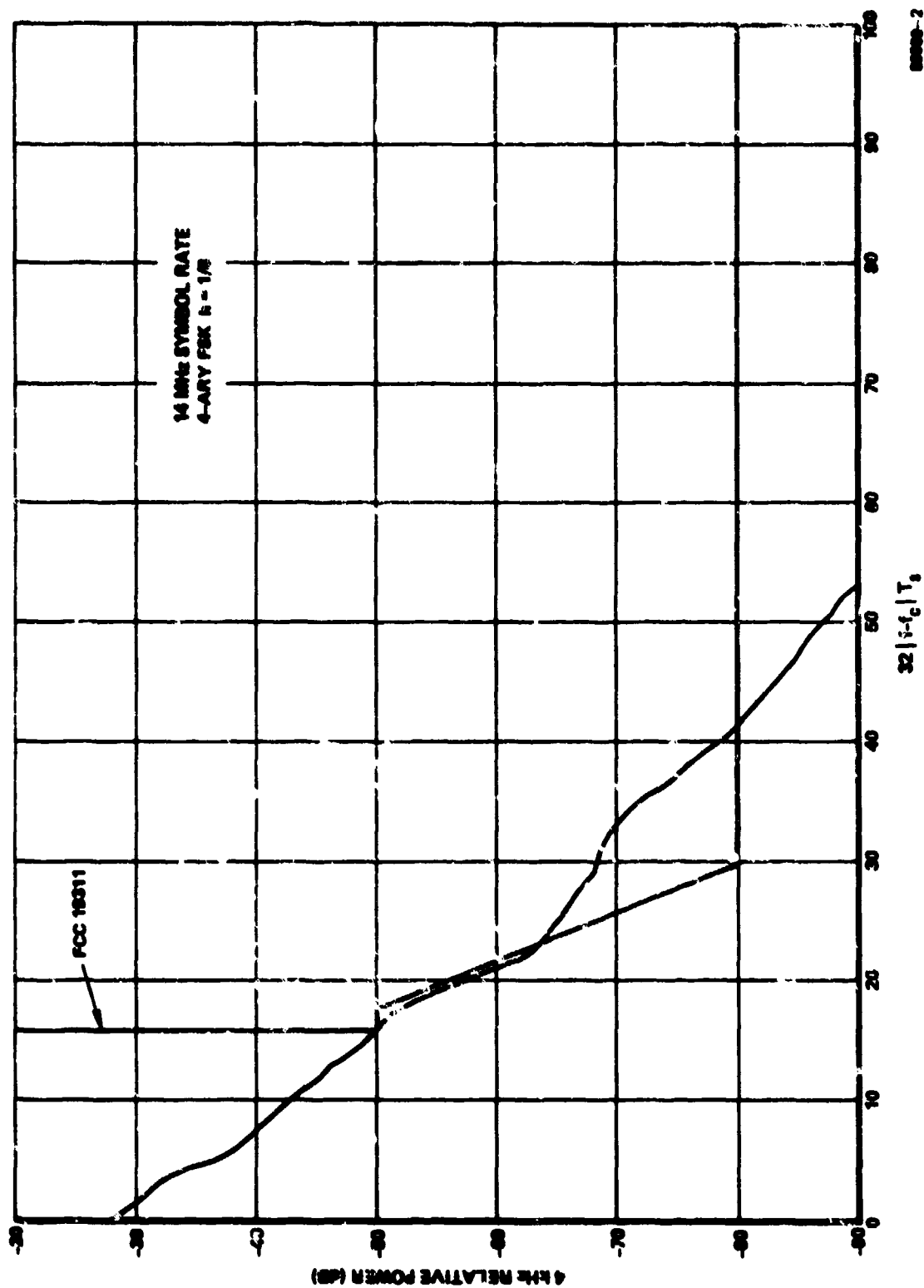
Figure 4. Eight-Pole, 18-MHz BW, 0.1 dB Tchebycheff Filtering

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net gain of only 7 dB over the prefilter level. This ineffectiveness at reducing the major side lobe was found to hold for all filters that insignificantly filtered the main lobe of the spectrum.

The reason for this is clear in retrospect based on the fact that the main lobe inside the authorized bandwidth contains 99 percent of the signal power. Filtering that leaves this lobe relatively untouched does not significantly distort or change the phase modulation of the original waveform. Since phase modulation is the only filtered signal characteristic that survives through the hard-limiter, it is then reasonable that the spectral side lobes would be restored to a large extent. Since such filtering affects only 1 percent of the total energy, it follows that only low level side lobes would be significantly reduced.

After observing these effects and in response to the argument above, it was concluded that only IF filters which filter the main lobe significantly had any hope of resulting in FCC 19311 compliance. The necessity for such bandwidth restrictive filters of course implies performance degradation due to additional intersymbol interference.

From previous computer simulations evaluating the effect of filters on FSK signals, it was felt that small group delay distortion would be of paramount importance in holding performance degradation to acceptable levels. At this point in the IF filter investigation, various perfectly phase compensated filters as well as Bessel filters (which have very low group delay distortion characteristics) were analyzed. Figures 5 and 6 show the spectra obtainable with 4-pole and 8-pole Bessel filters respectively when followed by hard limiting. The 4-pole filter 3 dB bandwidth is 0.3 times bit rate while for the 8-pole filter, a 0.33 times bit rate bandwidth is used. Rough calculations of performance indicated approximately 2 dB loss in performance relative to the previous breadboard modem.

Figure 7 shows the spectrum obtained with an IF filter with sinc function (sinc(x) ≈ sin(x)/X) rolloff out to the first null at ±0.75 symbol rate. The -3 dB bandwidth of this filter is 0.331 times bit rate. Rough calculations indicated a little less than 2 dB degradation with this filter relative to the previous breadboard.

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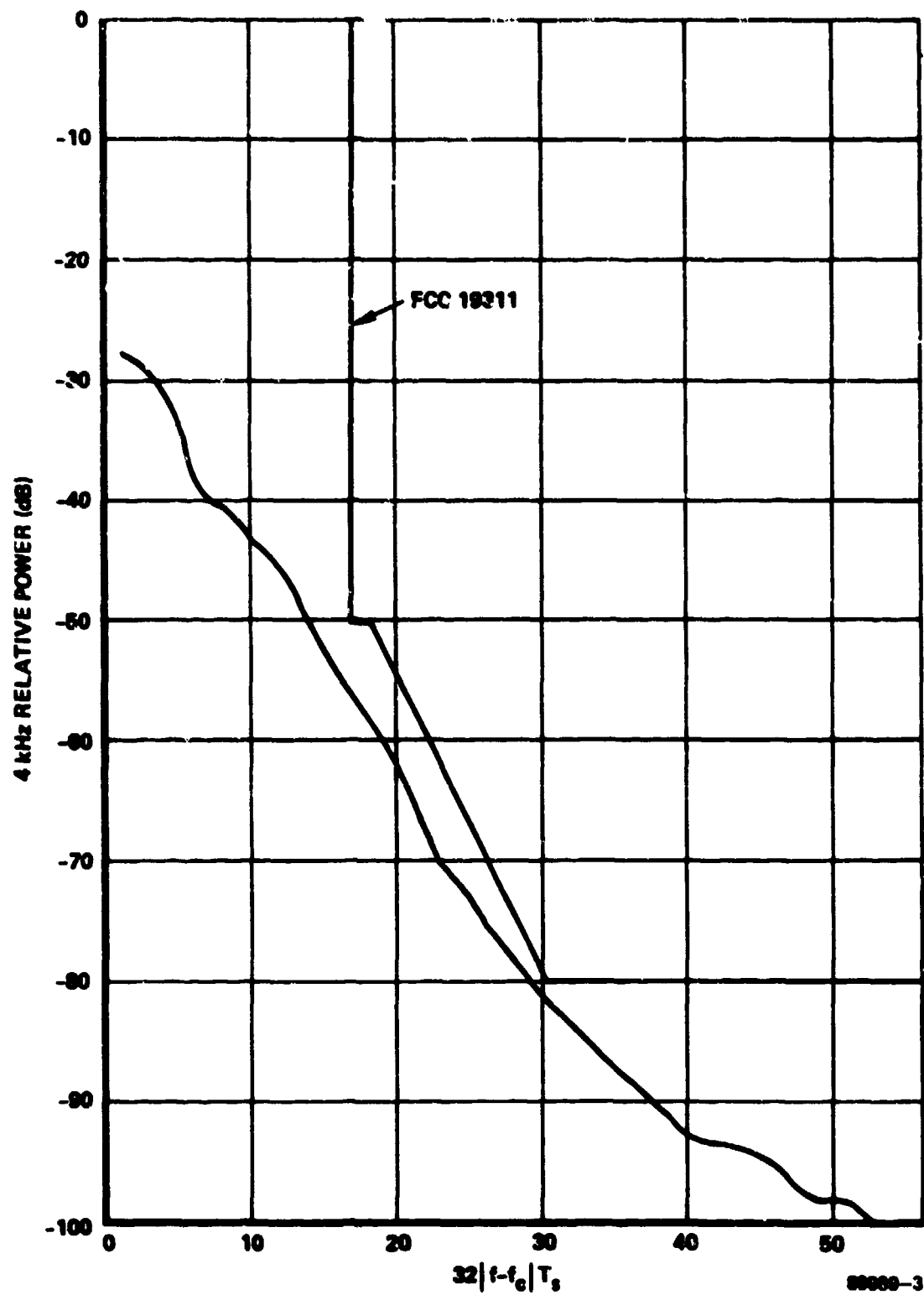
Figure 5.   Four-Pole, 0.3X BR BW, Bessel Filtering

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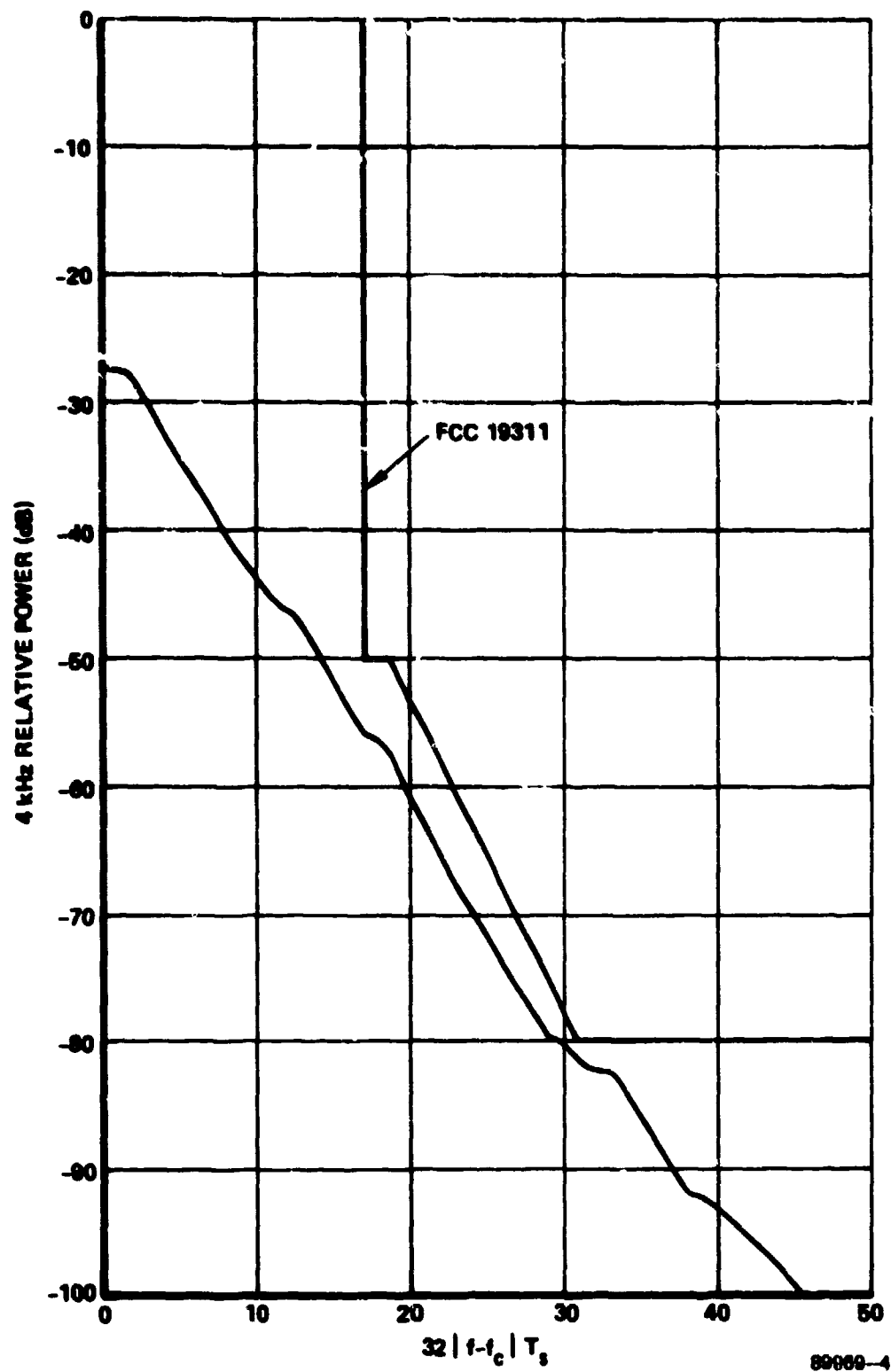
Figure 6. Eight-Pole, 0.33X BR BW, Bessel Filtering

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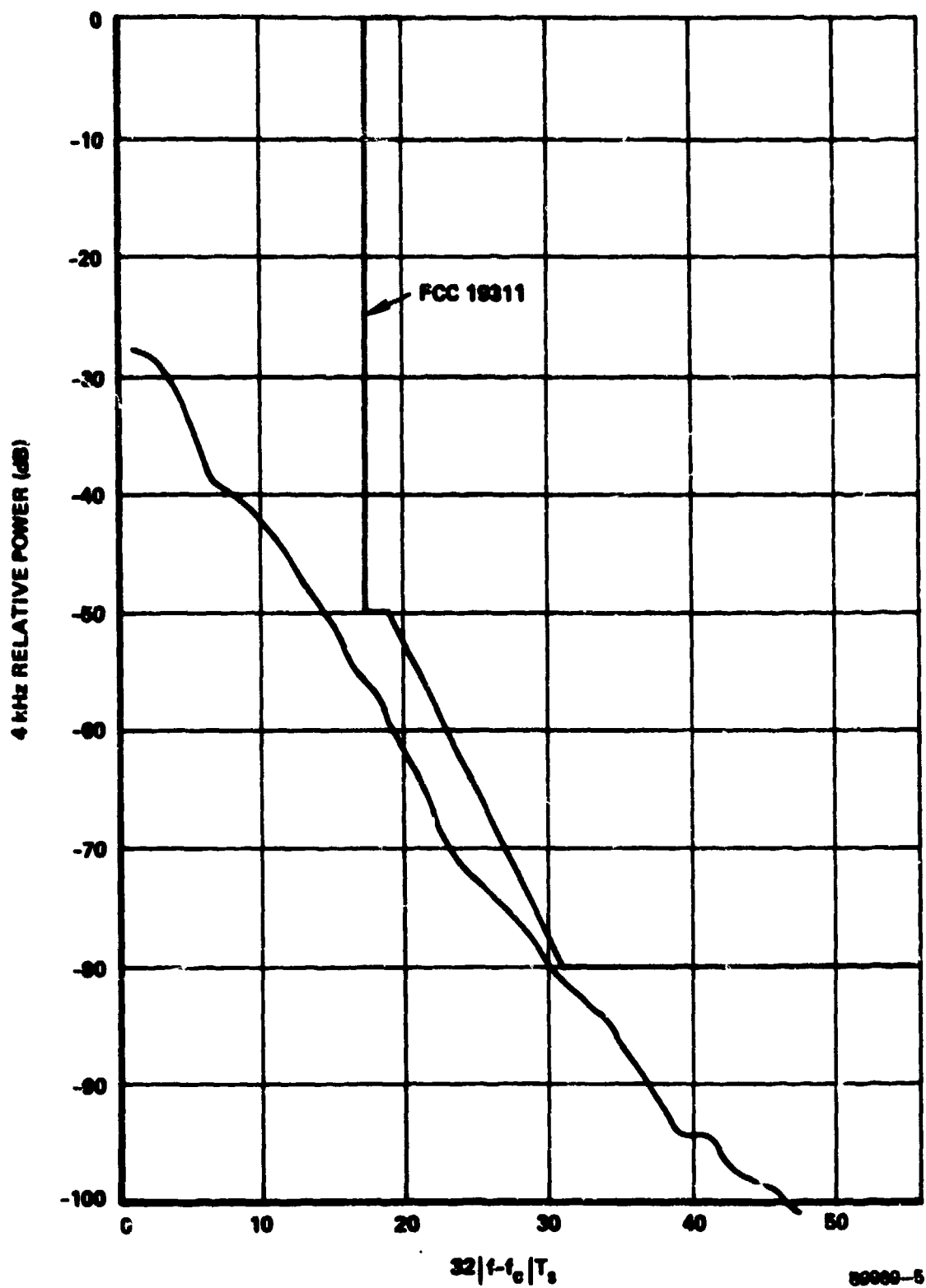
Figure 7. Sinc Rolldown (±0.75 SR)

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From these results, it was concluded that a 3 dB IF bandwidth of between 0.3 to 0.4 times bit rate would be required to meet FCC 19311 with an IF filter/limiter approach. Also, the rolloff outside the 3 dB bandwidth should be rapid-like the sinc function.

In an attempt to approximate the rapid rolloff and linear phase characteristic of the sinc function filter, performance and spectrum was examined with the filter shown in Figure 8. Here a 4-pole Butterworth filter with 3 dB bandwidth equal to symbol rate and with two sections of all-pass phase compensation is included. The filter's primary function is to
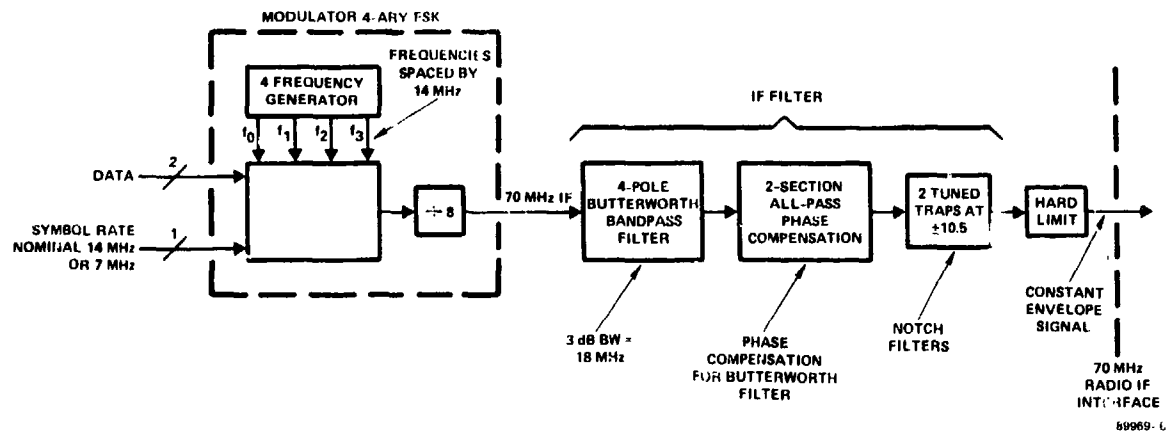
Figure 8. IF Filter Approach to FCC 19311

reduce higher order side lobes. The most significant main lobe filtering is done by the two tuned traps (zeros on j ω axis) at ±0.75 x symbol rate relative to carrier. These two zeros lead to parabolic frequency response between the two notch frequencies. The zeros also have the merit of theoretically creating no group delay distortion between the two notch frequencies. The overall attenuation and group delay distortion of this composite IF filter is shown in Figure 9. The 3 dB bandwidth of the filter is 0.375 x bit rate. This composite filter was used as the baseline in the

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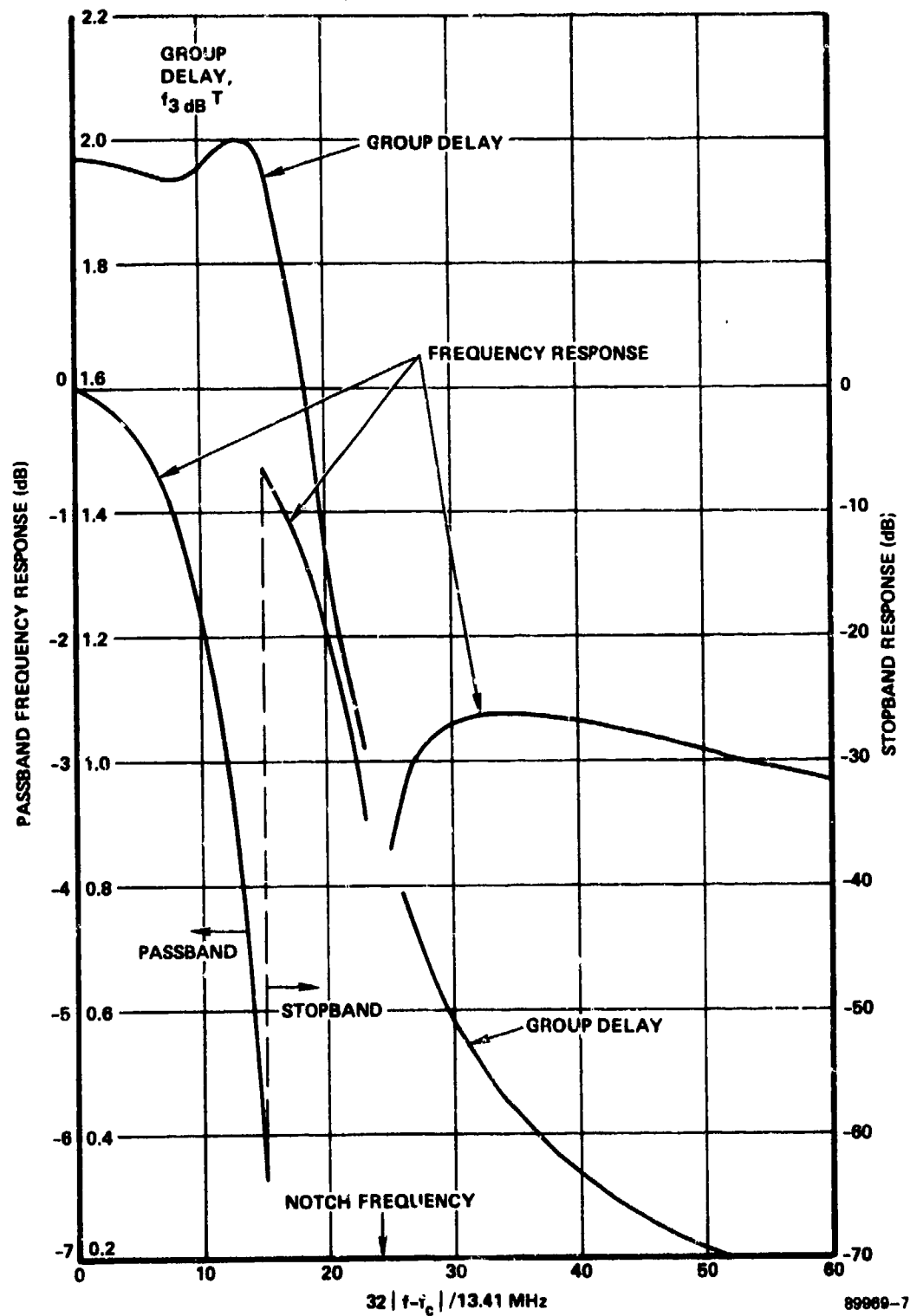
Figure 9. IF Approach Transmit Filter Characteristics

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following results for the IF filter approach to FCC 19311 compliance. The radiated signal spectrum using this IF filter for 2 B/Hz operation is shown in Figure 10. The radiated signal spectrum for 1 B/Hz operation is shown in Figure 11. Both modes use the same IF filter and both operate in an authorized bandwidth of 1 MHz.

Figure 12 shows the computer performance predictions for the IF filter baseline approach. The nominal baseline conditions are given in Table 1.

The 2 B/Hz mode theoretically requires 23.1 dB E_b/N_0 for a 5 x 10^{-9} symbol error rate.

Figure 13 shows the variation in symbol error rate as the symbol timing at the demod varies.

Figure 14 shows the variation in symbol error rate as the threshold spacing in our demod crosstalk correction algorithm changes.

The sensitivities shown on these figures are roughly the same degree of sensitivity to imperfections as the prior breadboard modem. However, the performance with the IF filter approach shown in Figure 12 is approximately 2.3 dB worse than the performance of the waveguide filter approach presented in the following section. Consequently, the IF filter approach was discarded in favor of using the waveguide filter. The IF filter bandwidth required for FCC 19311 compliance was simply too narrow and resulted in excessive signal distortion relative to the waveguide filter approach.

At the end of the study phase it was discovered that the simulation which produced the performance curve for the IF filter approach shown in Figure 12 was producing optimistic predictions. Due to time limitations these simulations were not re-run. In any case, the trade-off between IF and waveguide filtering is weighted even more toward the waveguide approach.
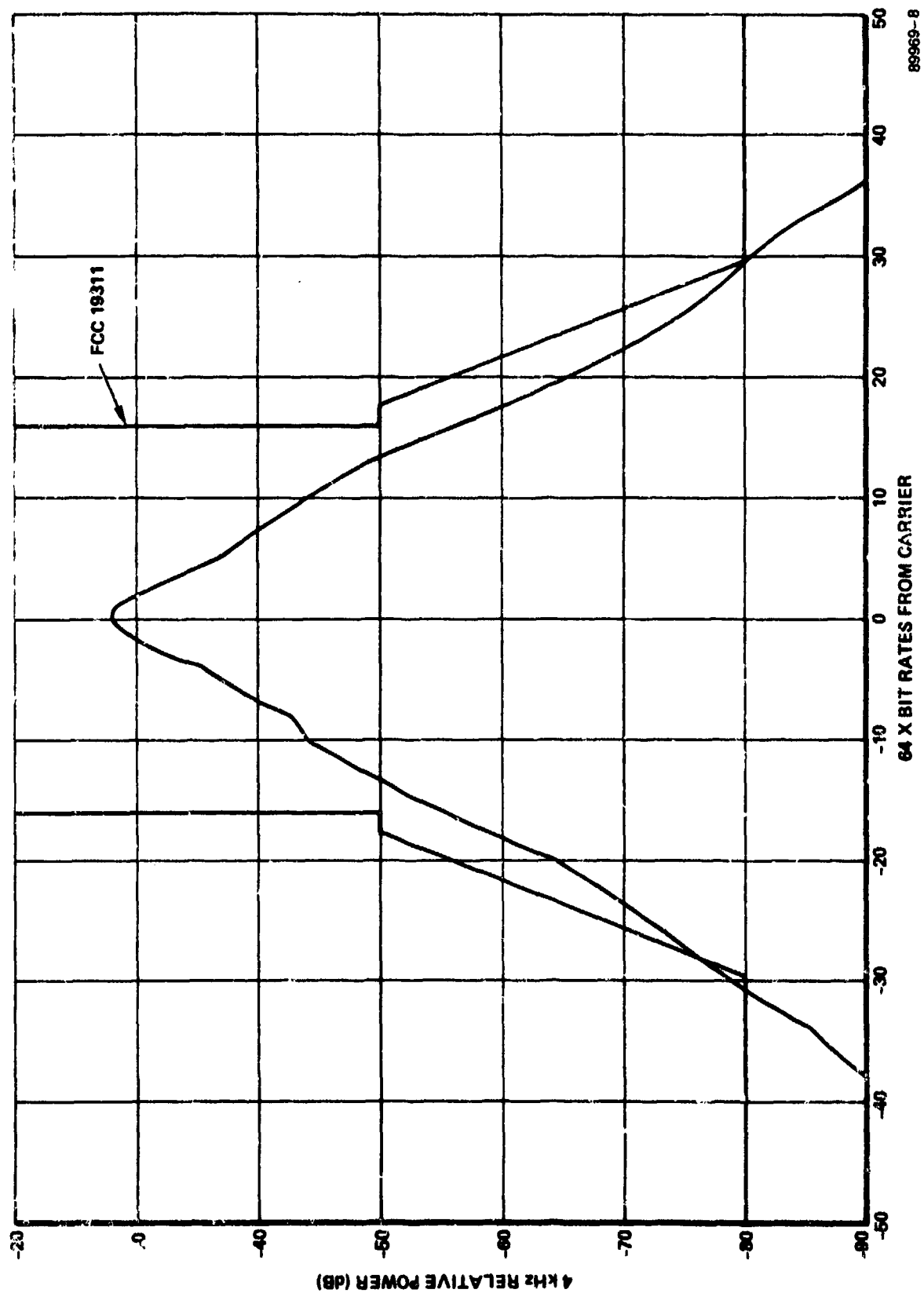
Figure 10. IF Approach 2 B/Hz Spectrum

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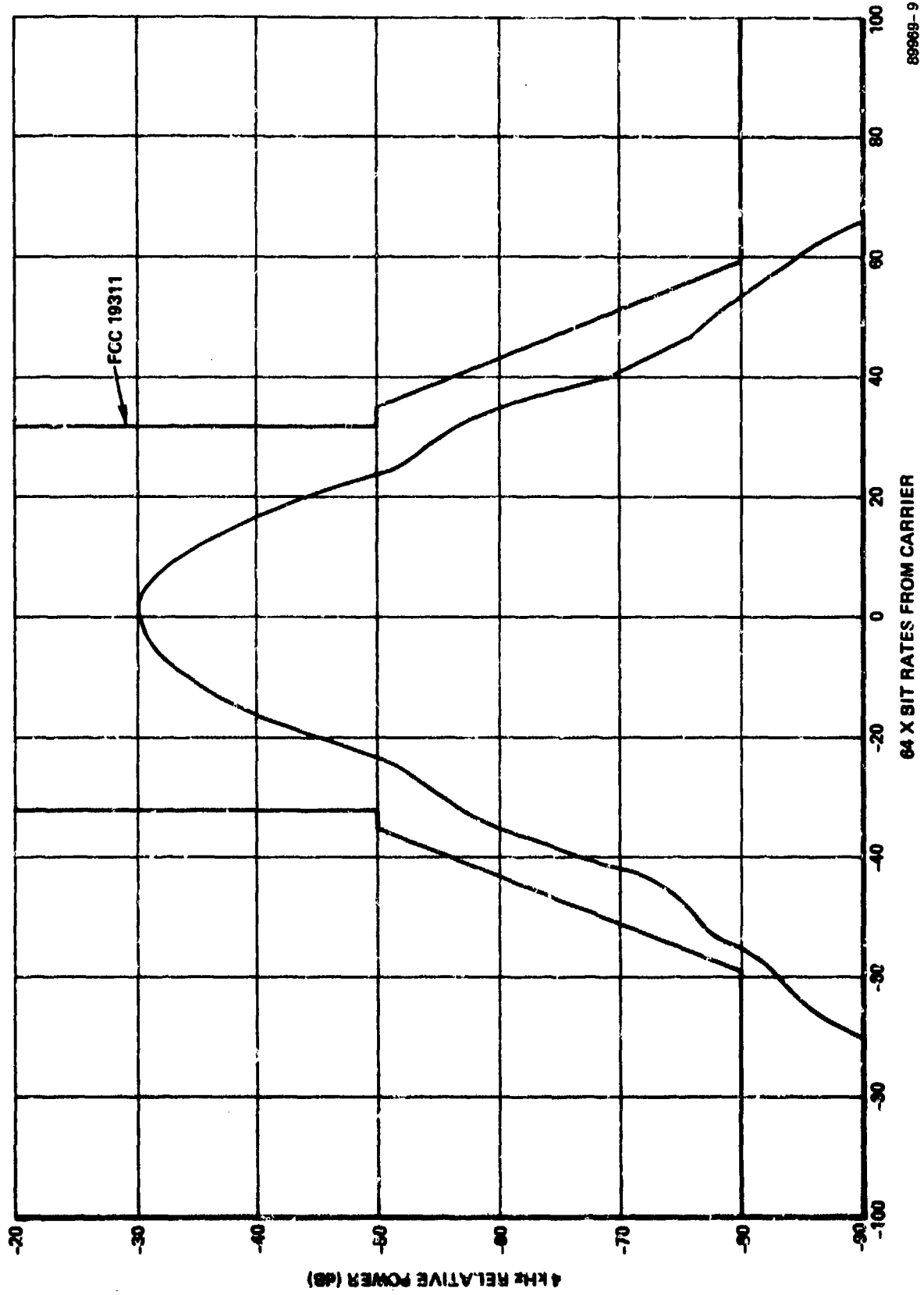
Figure 11. IF Approach 1 B/Hz Spectrum

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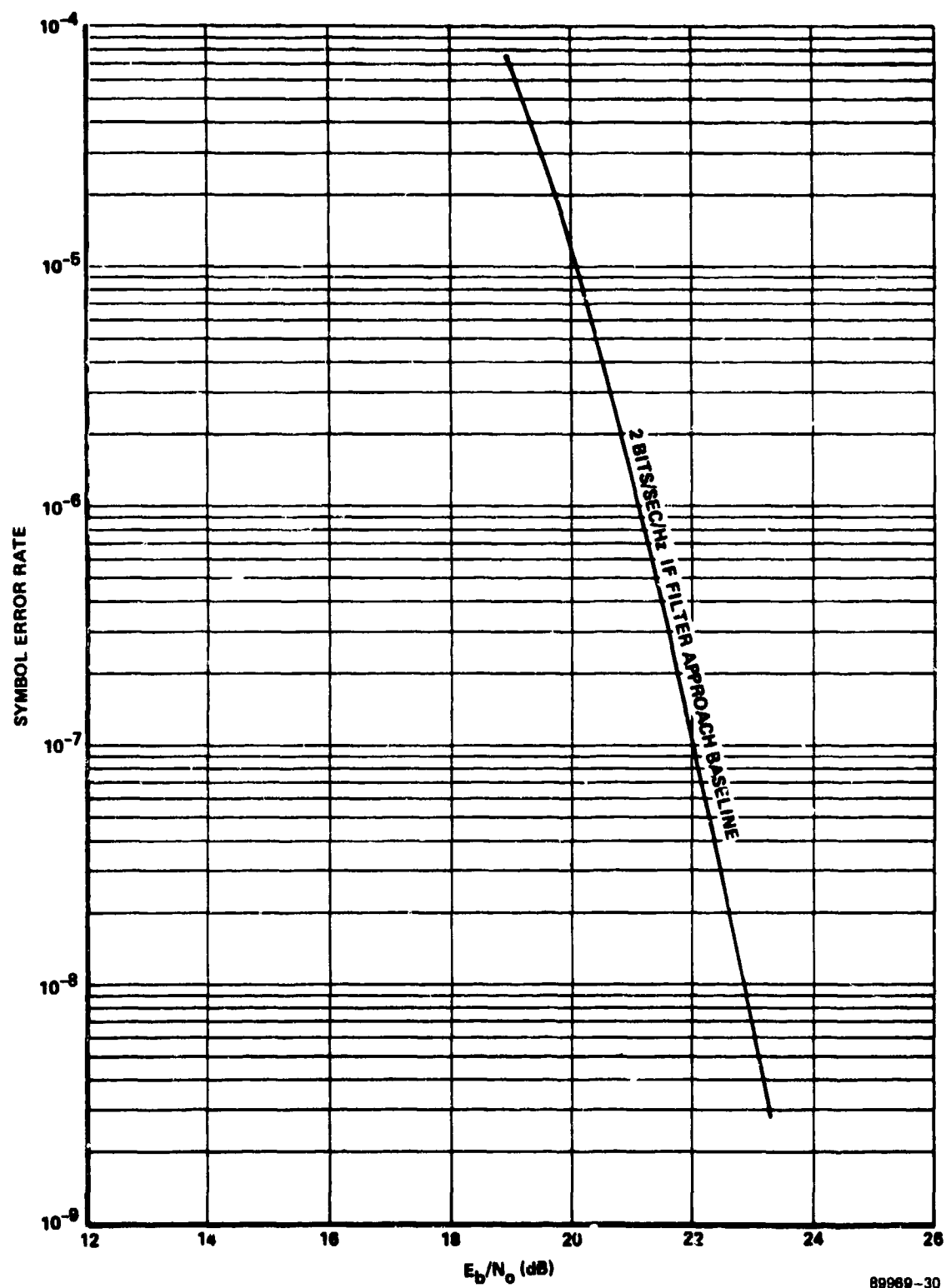
Figure 12.   IF Filter Approach Performance

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Table 1. Nominal Baseline Conditions for IF Approach

1. **TRANSMIT IF FILTER:** 4-pole Butterworth with 3 dB bandwidths of 13.41 MHz and containing two section all-pass phase compensation. Two tuned traps at 70 10.05 MHz.

2. **RADIO TRANSMIT IF FILTERS:** 3-pole 0.1 dB ripple Tchebycheff and 3-pole Butterworth both with 3 dB bandwidths of 30 MHz.

3. **DEMOD IF FILTER:** 4-pole Butterworth with 3 dB bandwidths equal to symbol rate and containing two section all-pass phase compensation.

4. **CROSSTALK ALGORITHM THRESHOLD SETTING:** $\theta = 5.5^O$.

5. **REFERENCE LOOP PHASE JITTER:** 0.7^O rms.

6. **SYMBOL TIMING:** Within 1 percent of symbol time of best location.

2.3.1.2 Waveguide Filter Approach

In this section the study effort which considered the use of microwave waveguide filters for spectral shaping to meet FCC 19311 is presented.

2.3.1.2.1 Filter Characteristics

The nominal center frequency of the Philco LC8D radio used for testing the modem was 8.075 GHz. The filter attenuation characteristic needed for FCC 19311 compliance is primarily dictated by the 18 dB violation of the spectral mask for 2 B/Hz at symbol rate (one-half bit rate) removed from carrier. For this modem the nominal bit rate is 26.82 Mb/s. Thus the waveguide filter is centered at 8.075 GHz and must be at least 18 dB down at ±13.41 MHz. Based upon computer simulations and consideration of waveguide filter types readily available in the industry, it was decided to use a 4-pole Butterworth filter with 3 dB bandwidth of 16 MHz for this approach. The use of such a filter results in near-optimum

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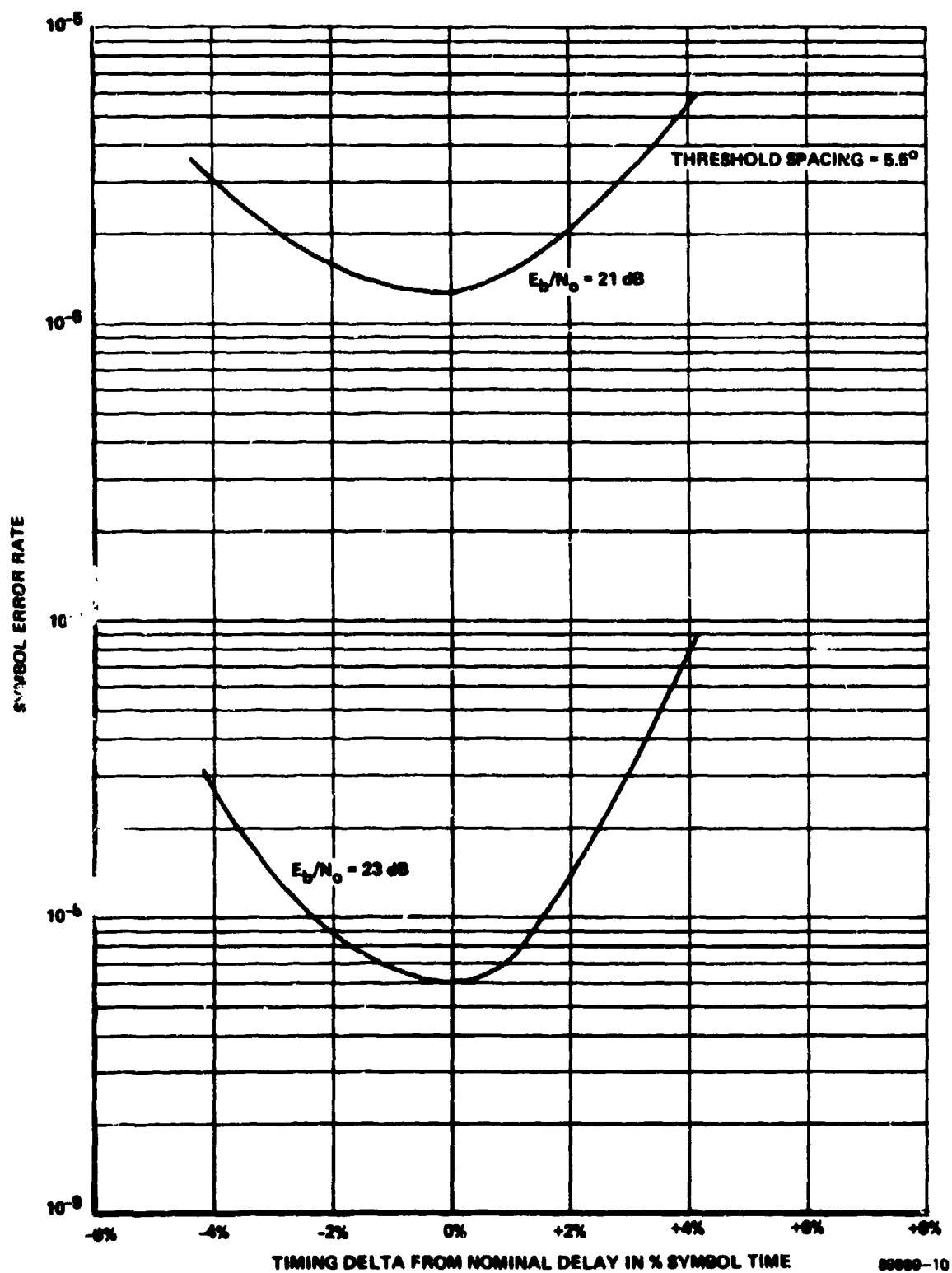
Figure 13. Nominal IF 19311 Approach Timing Sensitivity

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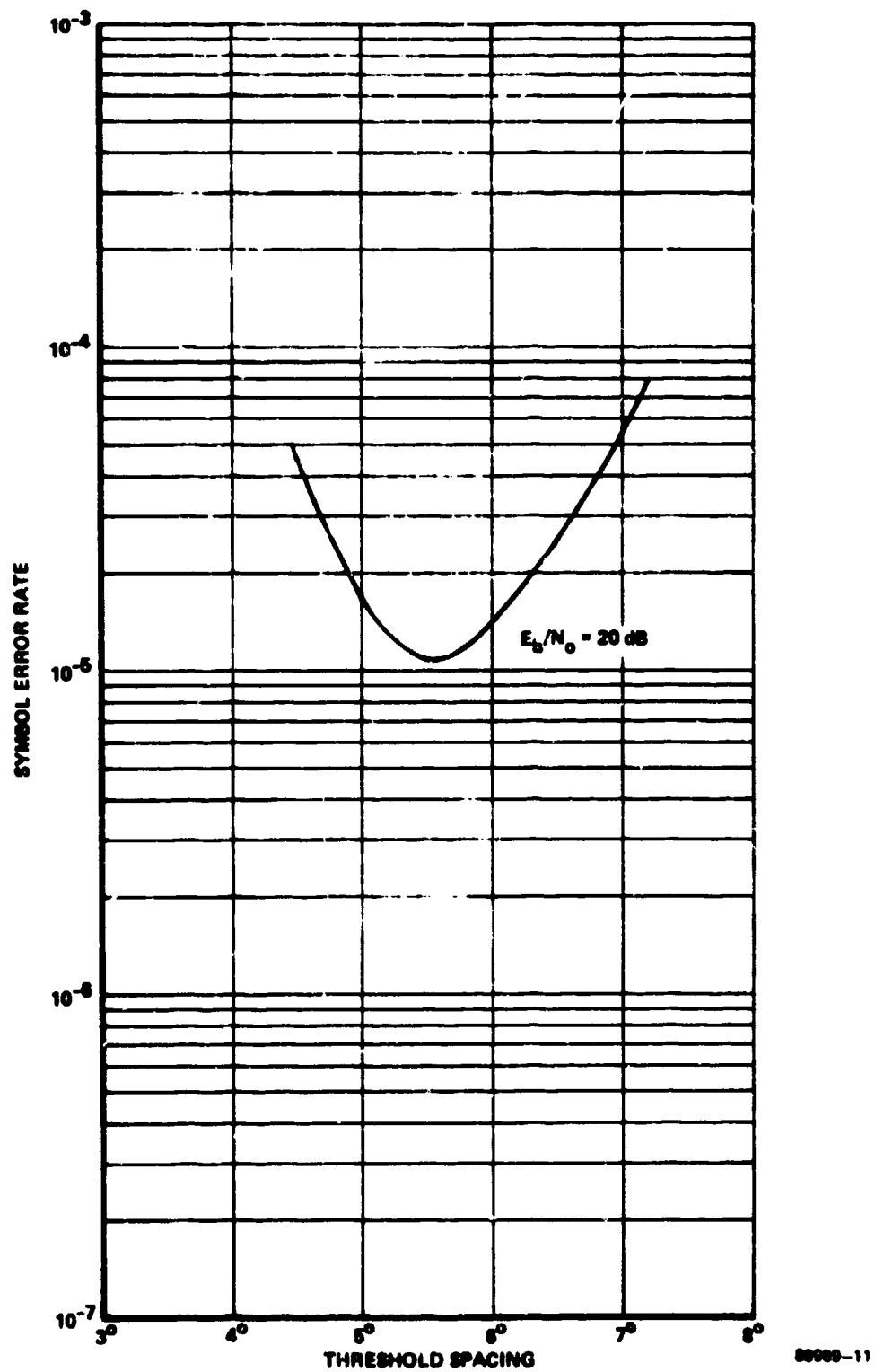
Figure 14. Nominal IF 19311 Approach Threshold Spacing Sensitivity

performance and leads to FCC 19311 compliance for both the 2 B/Hz and
1 B/Hz modes operating in an authorized bandwidth of 14 MHz. The
attenuation and group delay distortion for this filter are shown in Figures
15 and 16 respectively. When the baseline radio filters are included, the
overall attenuation and group delay characteristics are as shown in Figures
17 and 18 respectively.

Discussions with waveguide filter manufacturers (Microwave
Development Laboratories (MDL) and Wavecom) revealed that INVAR
construction of such a filter will lead to ±400 kHz of center frequency
detuning at 8 GHz and with ±25° C temperature variation. This detuning
number results from assuming INVAR material has a temperature coefficient
of expansion of $2 \times 10^{-10}/°$ C. The formula indicated by MDL for
computing detuning is

$$D = \epsilon f_c (\Delta T) \tag{1}$$

where D = Frequency detuning.

            ϵ = temperature coefficient of expansion.

            f_c = filter center frequency.

            ΔT = temperature variation.

The assumption of ±25° C operating temperature variation is supported by
reference to DRAMA specs (0° to 49° C) and to the Philco LC8D radio
specs (0° to 50° C). Equation (1) then indicates

$$D = 2 \times 10^{-6} \times 8 \times 10^6 \times (\pm 25) \text{ kHz}$$

or $D = \pm 400$ kHz

2.3.1.2.2   Waveguide Filter Results

Figures 19 and 20 show the spectra obtained with the waveguide
filter for the 2 B/Hz and 1 B/Hz modes respectively. The effect of trans-
mitter detuning of ±402 kHz is indicated on these figures. This ±402 kHz
frequency variation is the amount of detuning occurring in an 8 GHz wave-
guide filter of INVAR construction for a ±25° C temperature variation.
These figures show that the spectra both will meet the FCC 19311 masks for

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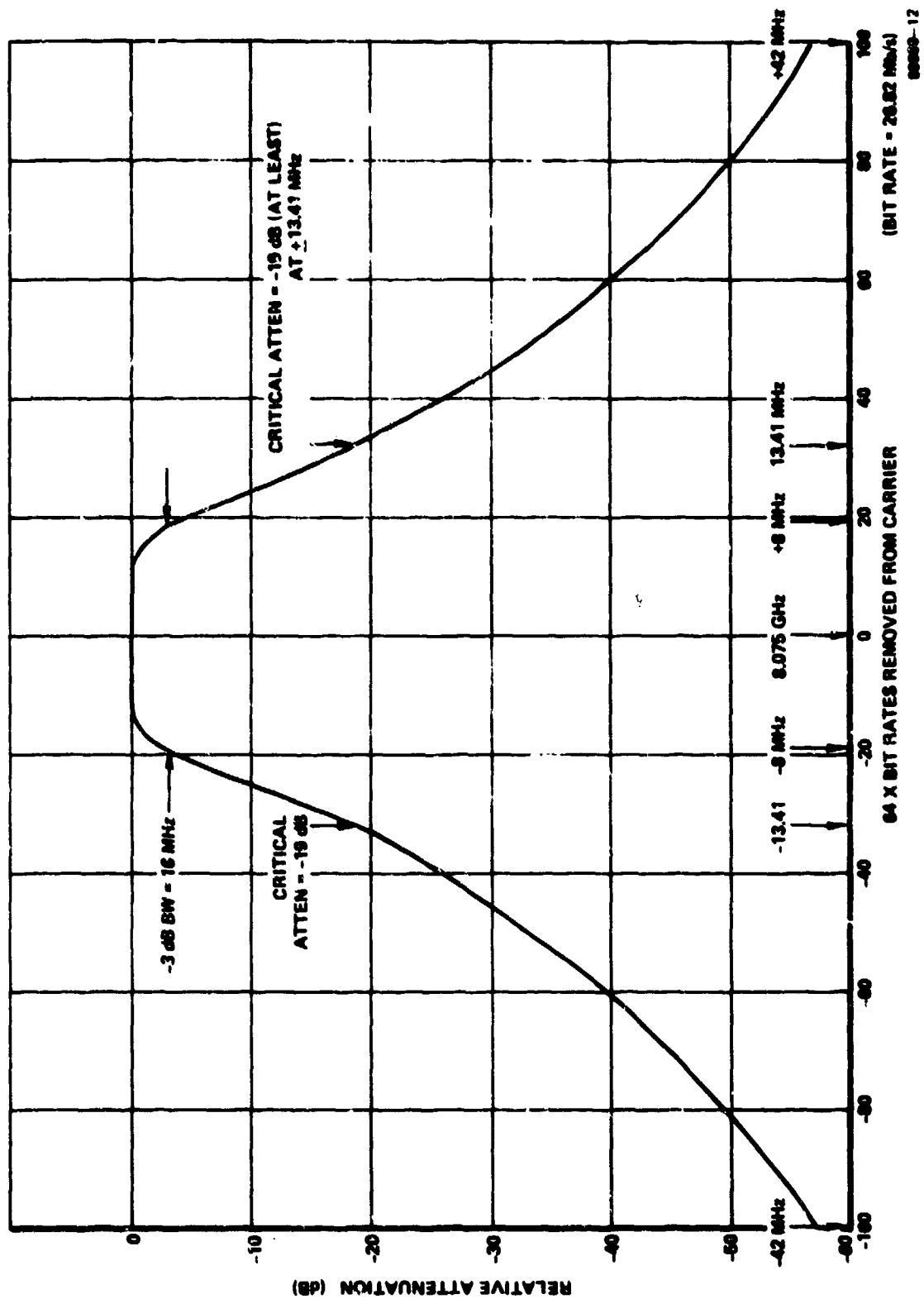
Figure 15.   Four-Pole Butterworth Waveguide Filter Attenuation Characteristics
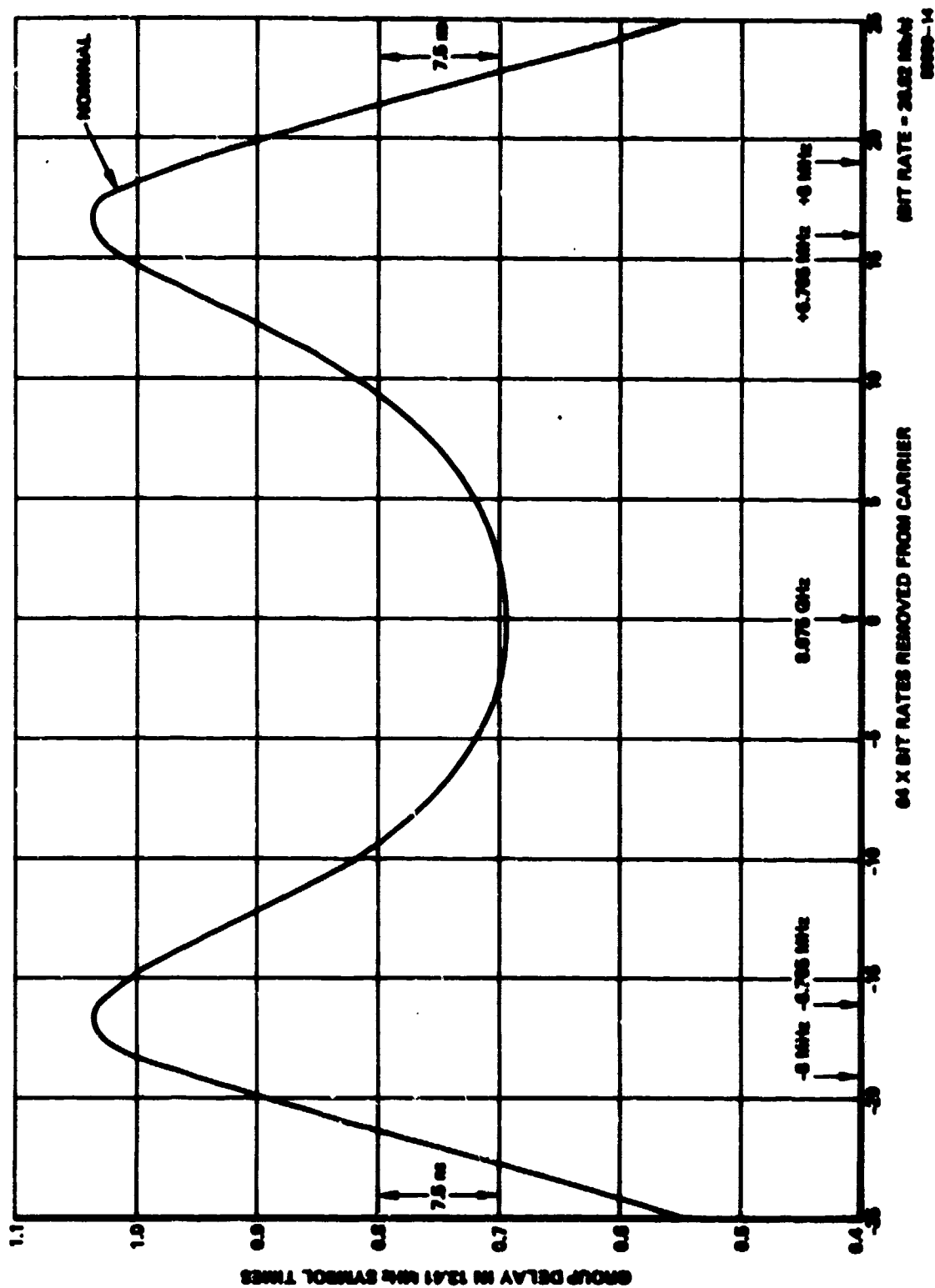
Figure 16. Four-Pole Butterworth Waveguide Filter Delay Distortion Characteristics
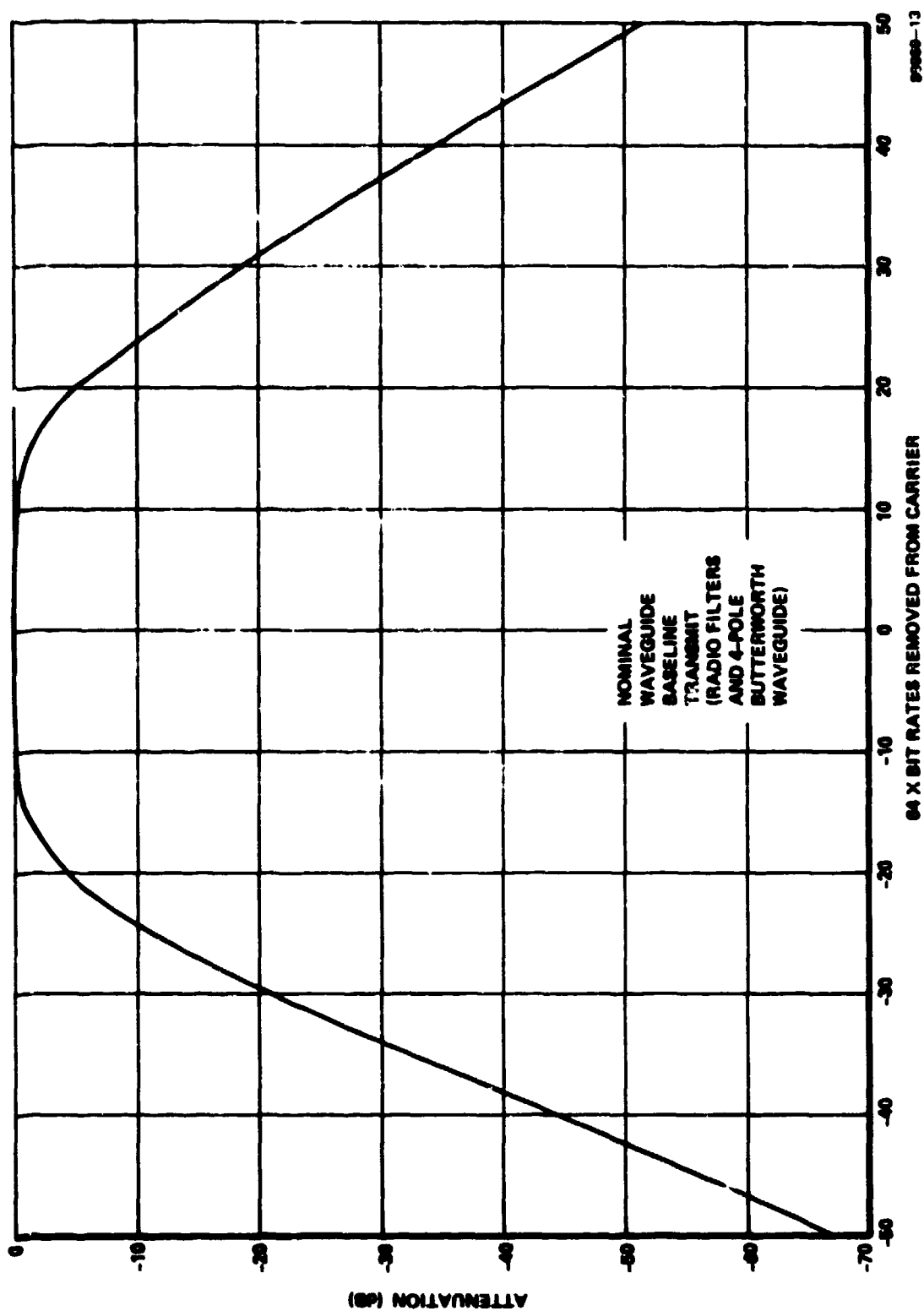
Figure 17. Nominal Waveguide Baseline Transmit Attenuation
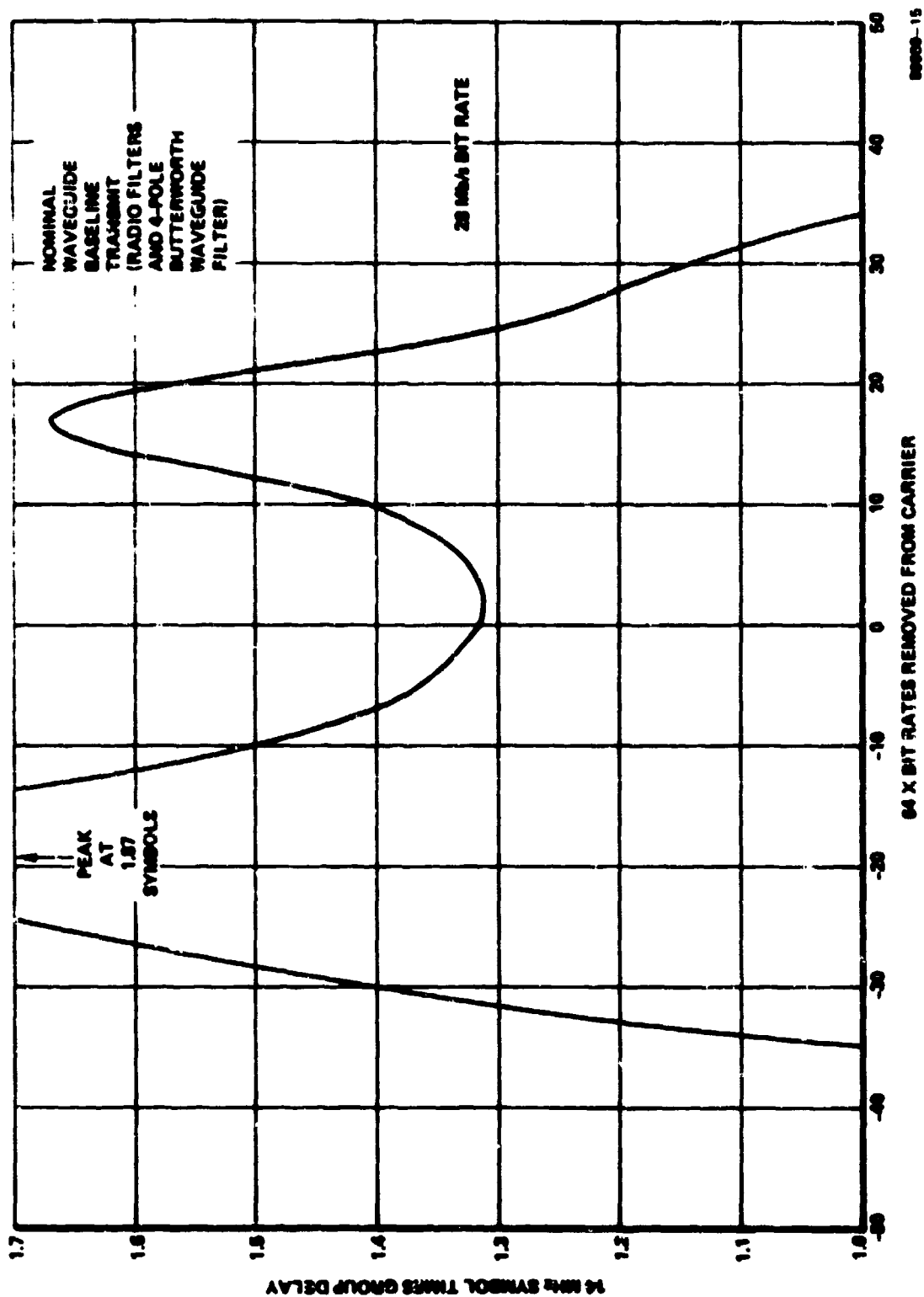
Figure 18. Nominal Waveguide Baseline Transmit Group Delay
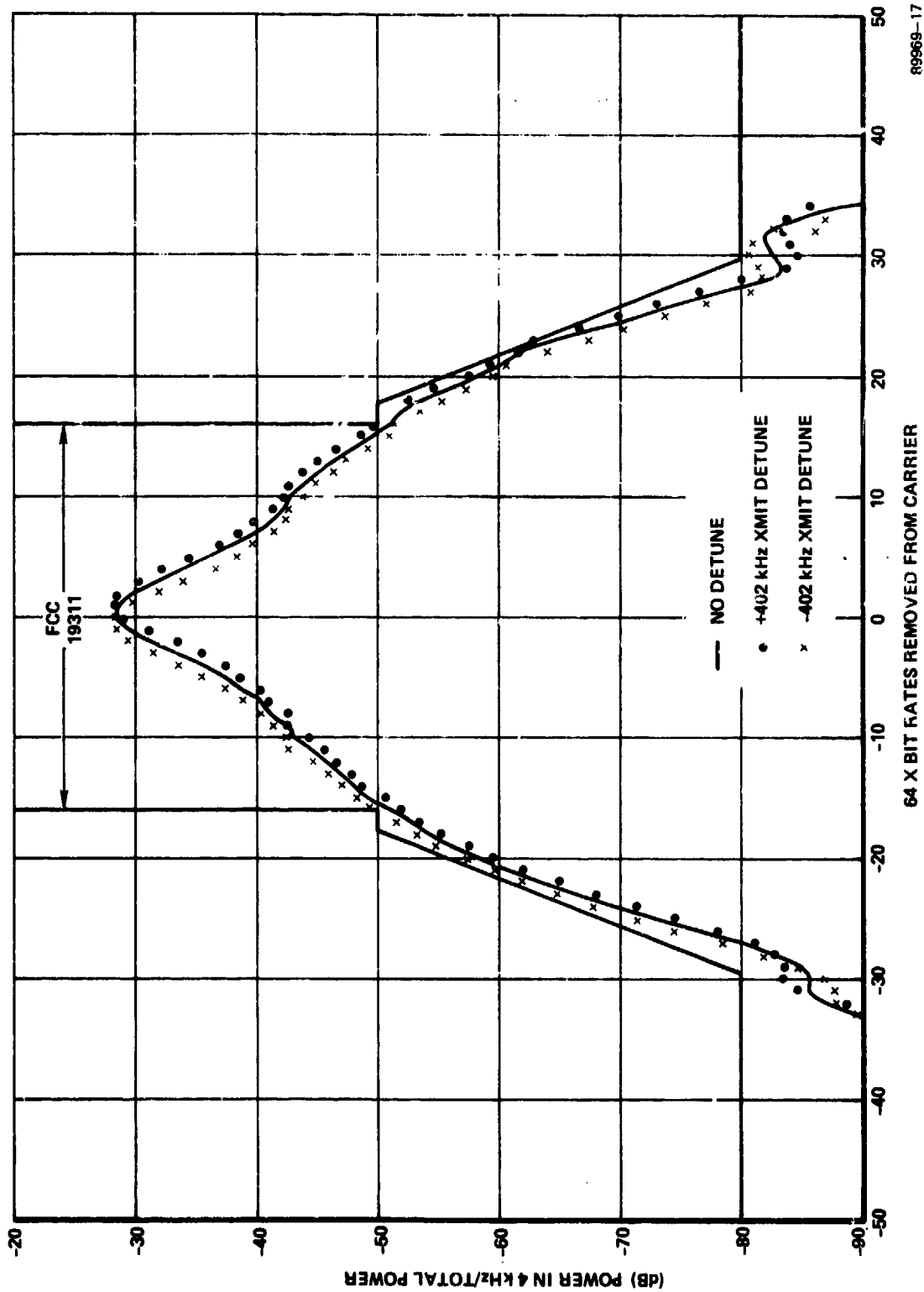
Figure 19. Waveguide Approach 2 B/Hz Spectrum

31
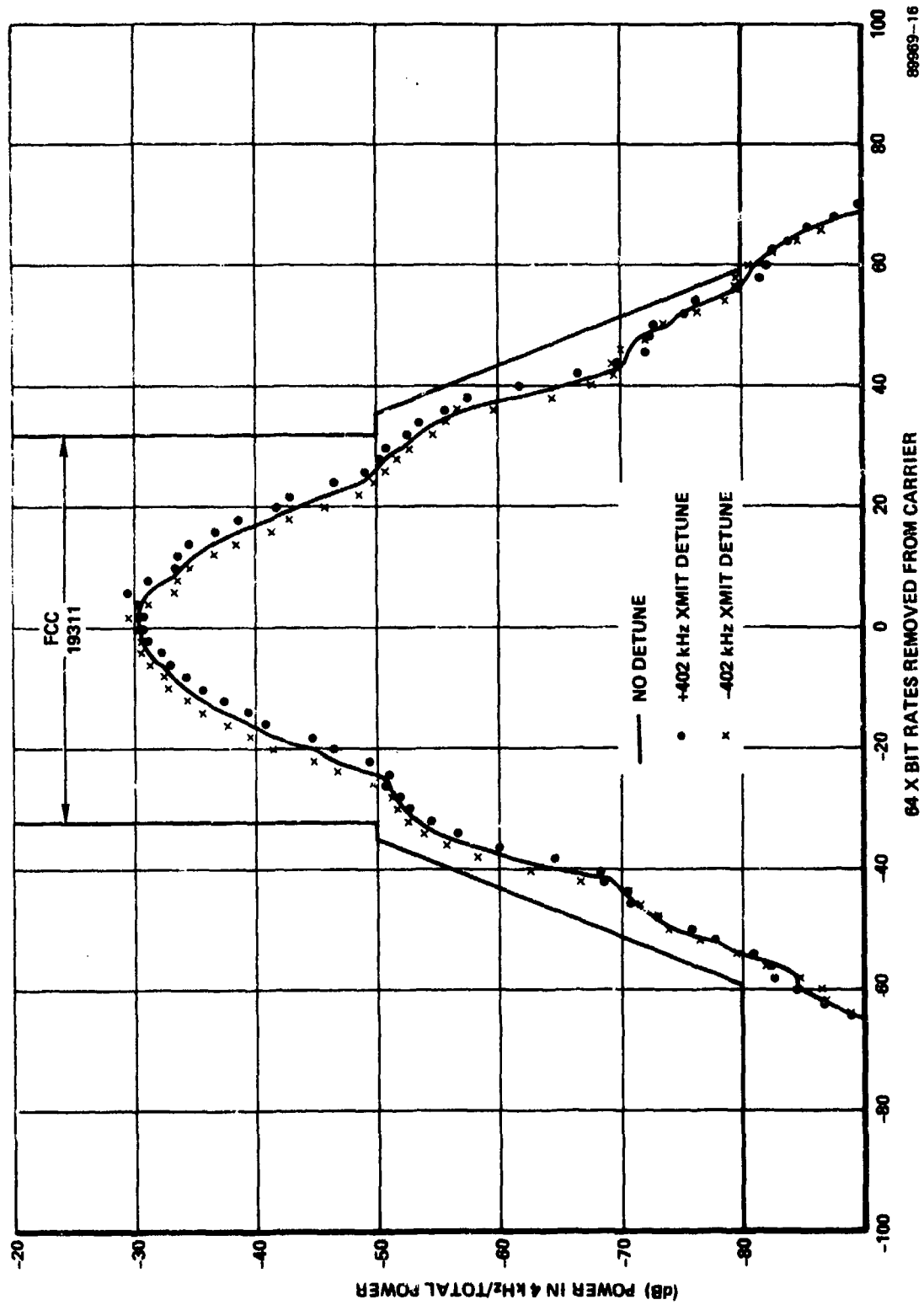
Figure 20. Waveguide Approach 1 B/Hz Spectrum

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$\pm 25^{\circ}$ C temperature variation with a waveguide filter of INVAR construction. It is impossible – both from performance and spectra viewpoints - to use non-INVAR construction since center frequency shifts an order of magnitude greater would occur (± 4 MHz) over this temperature range.

Figure 21 shows the performance for the waveguide filter baseline approach. The nominal conditions for the baseline are given in Table 2. As shown, 2 B/Hz operation at 5×10^{-9} error rate requires 20.8 dB E_b/N_o while 1 B/Hz operation requires 14.3 dB E_b/N_o. These predictions are roughly 3 dB better than the performance predicted for the IF filter approach. Figure 22 shows the performance of the modem back-to-back at IF, i.e., without the waveguide filter.

Figure 23 shows the variation of symbol error rate with detuning. This curve is important in comparing the detuning effect versus temperature for the waveguide filter against performance degradation to be expected. As indicated in Figure 23 the symbol error rate degrades by less than a factor of 2 for ± 402 kHz detuning. This represents less than 0.2 dB signal-to-noise degradation at a 5×10^{-9} bit error rate.

Figure 24 shows the variation of symbol error rate with changes in threshold spacing at the crosstalk algorithm.

Figure 25 shows the variation in symbol error rate with demod symbol timing variation.

Again, the indicated sensitivities to equipment imperfections is comparable to the previous breadboard sensitivities. Because of the better performance available with the waveguide filter approach to FCC 19311 spectral compliance, the waveguide was chosen for the baseline for this modem.

2.3.2   New Implementation Techniques

This section documents the study effort which investigated new implementation techniques for the modem. The effort centered primarily upon reconfiguring the phase detector reference derivation to eliminate critical phasing, timing, and acquisition problems encountered in the previous breadboard unit.

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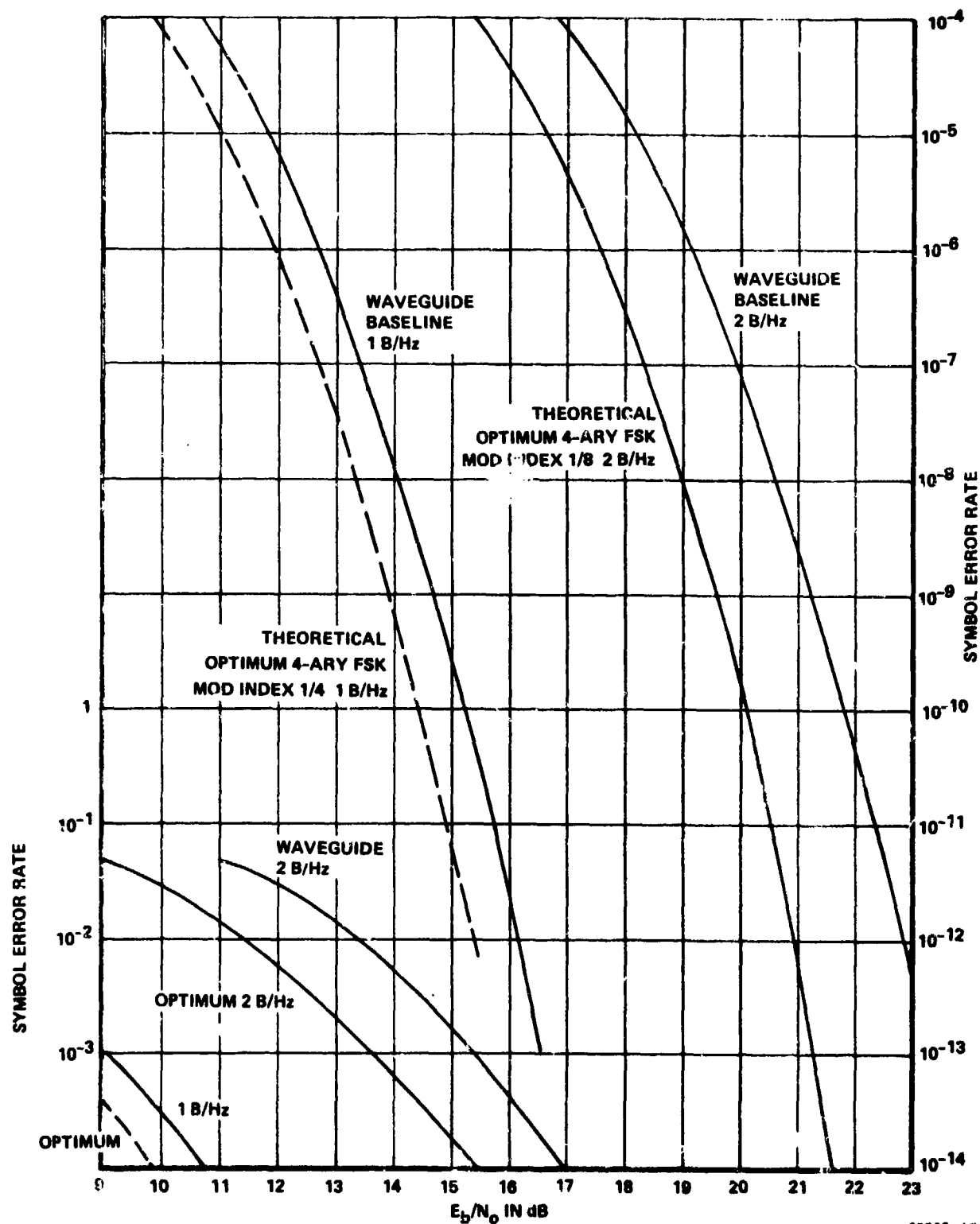
Figure 21. Waveguide Approach Baseline Performance

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Table 2. Nominal Baseline Conditions for Waveguide Filter Approach

1. RADIO TRANSMIT IF FILTER: 3-pole 0.1 dB ripple Tchebycheff and
                                  3-pole Butterworth - both with 3 dB
                                  bandwidths of 30 MHz.

2. WAVEGUIDE FILTER: 4-pole Butterworth with 3 dB bandwidth
                                  of 16 MHz.

3. DEMOD IF FILTER: 4-pole Butterworth with 3 dB BW equal to
                                  symbol rate containing two section
                                  all-pass phase compensation.

4. CROSSTALK ALGORITHM
    THRESHOLD SETTING: $\theta = 5^{\circ}$.

5. REFERENCE LOOP
    PHASE JITTER: 0.7° rms.

6. SYMBOL TIMING: Within 1 percent of symbol time of best
                                  location.

7. WAVEGUIDE FILTER
    DETUNING: 0.

35
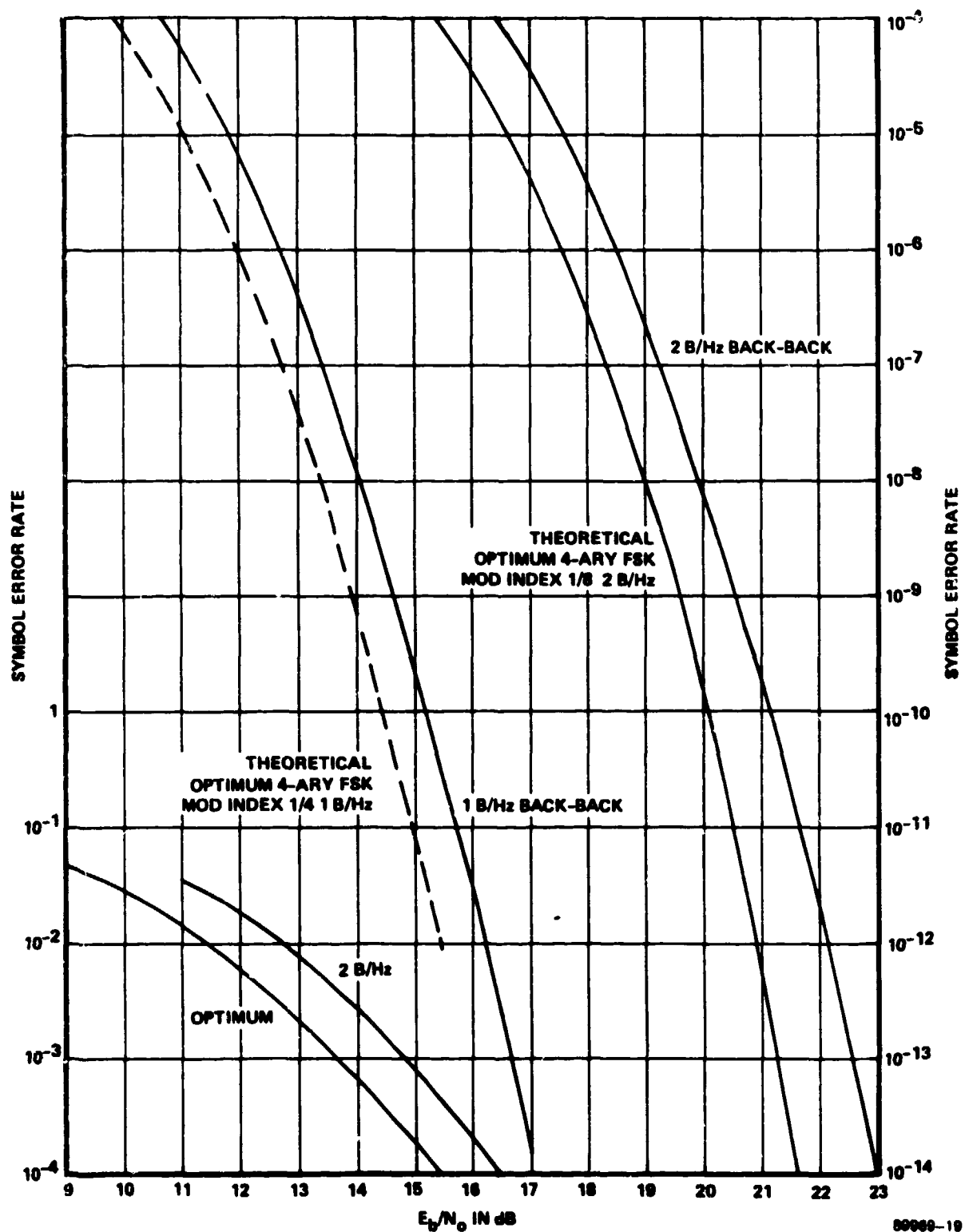
Figure 22. Back-to-Back Waveguide Baseline (Without Filtering)

36
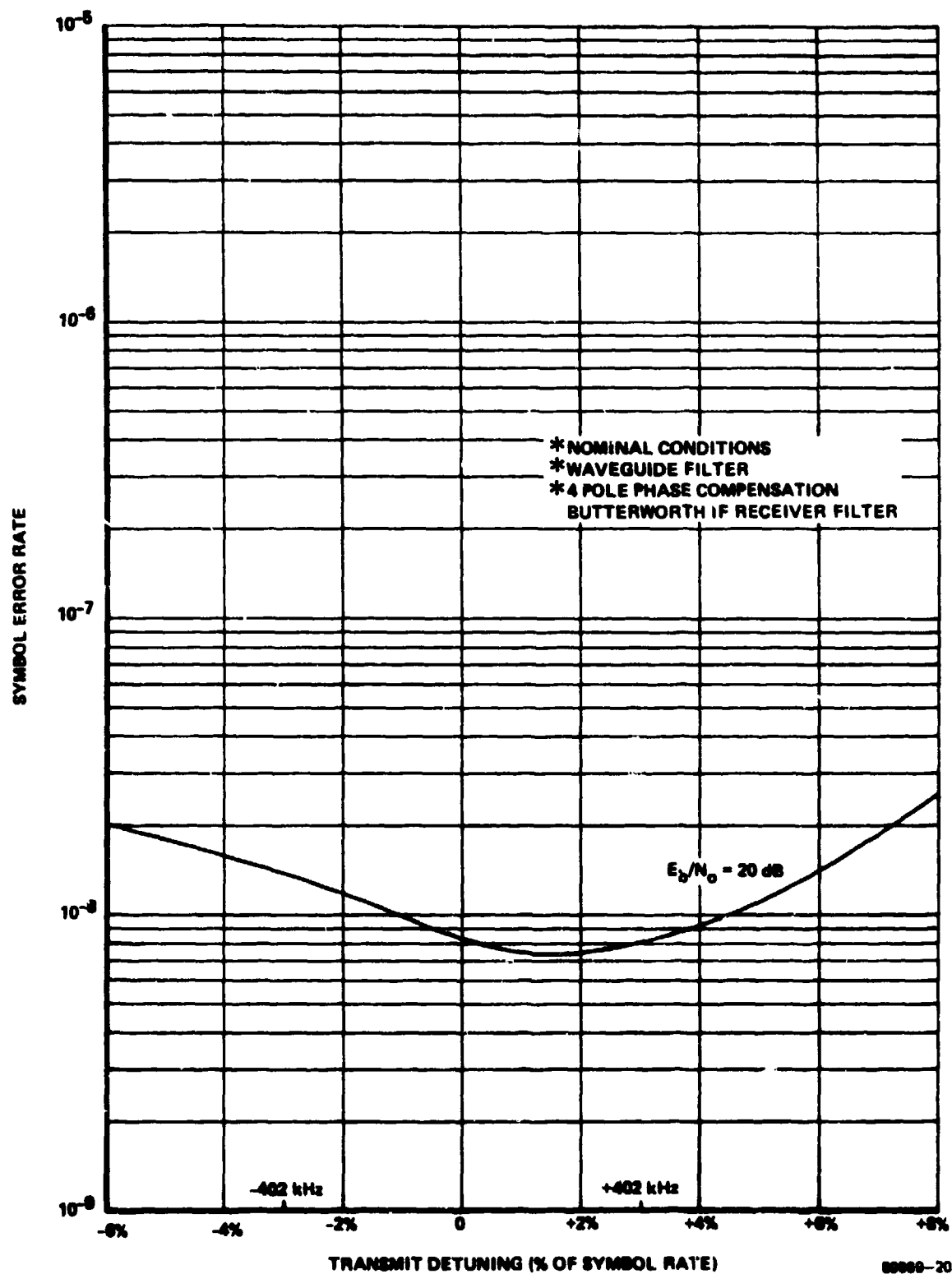
Figure 23. Waveguide Approach Detuning Sensitivity
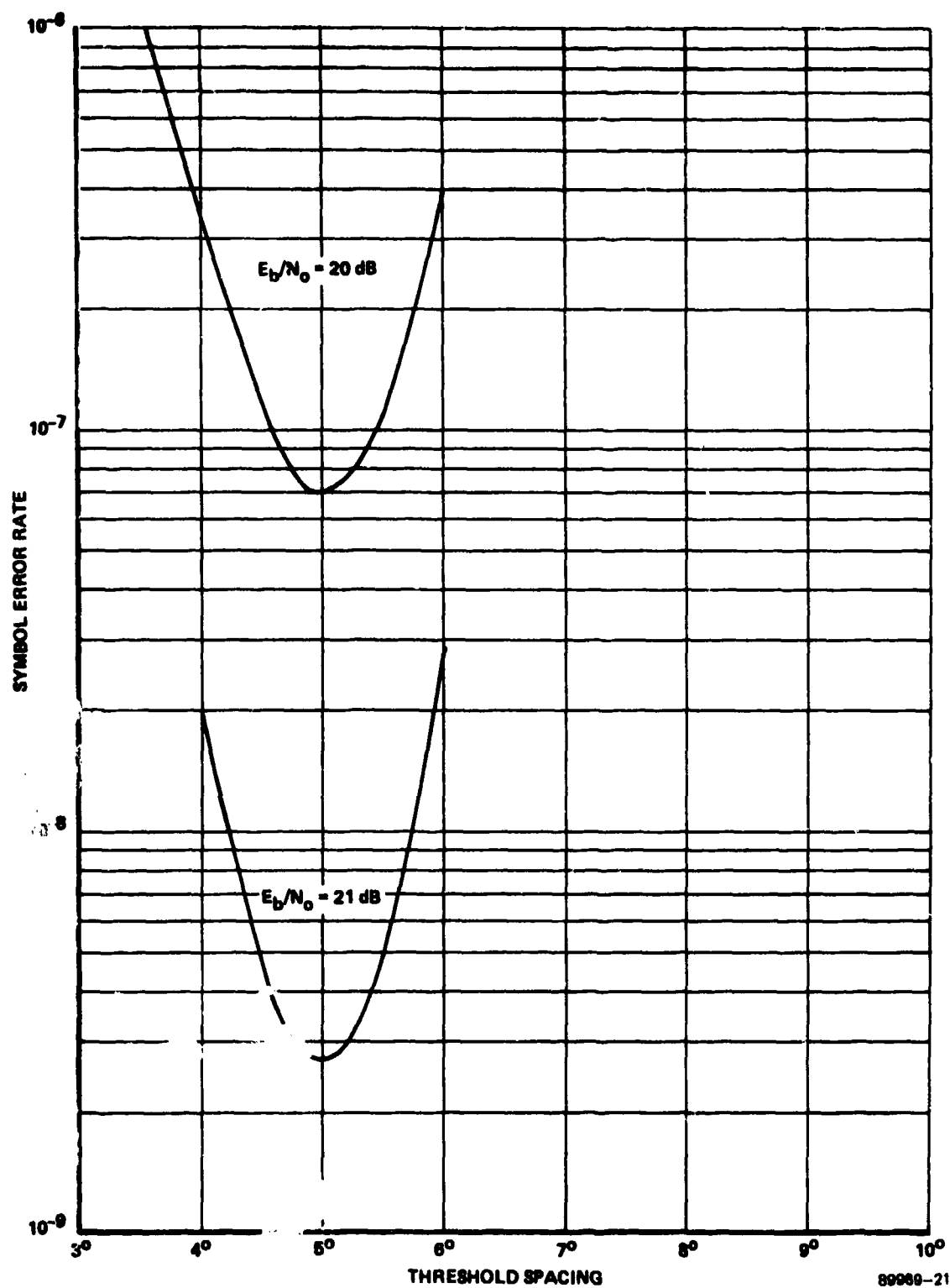
Figure 24. Waveguide Approach Threshold Spacing Sensitivity

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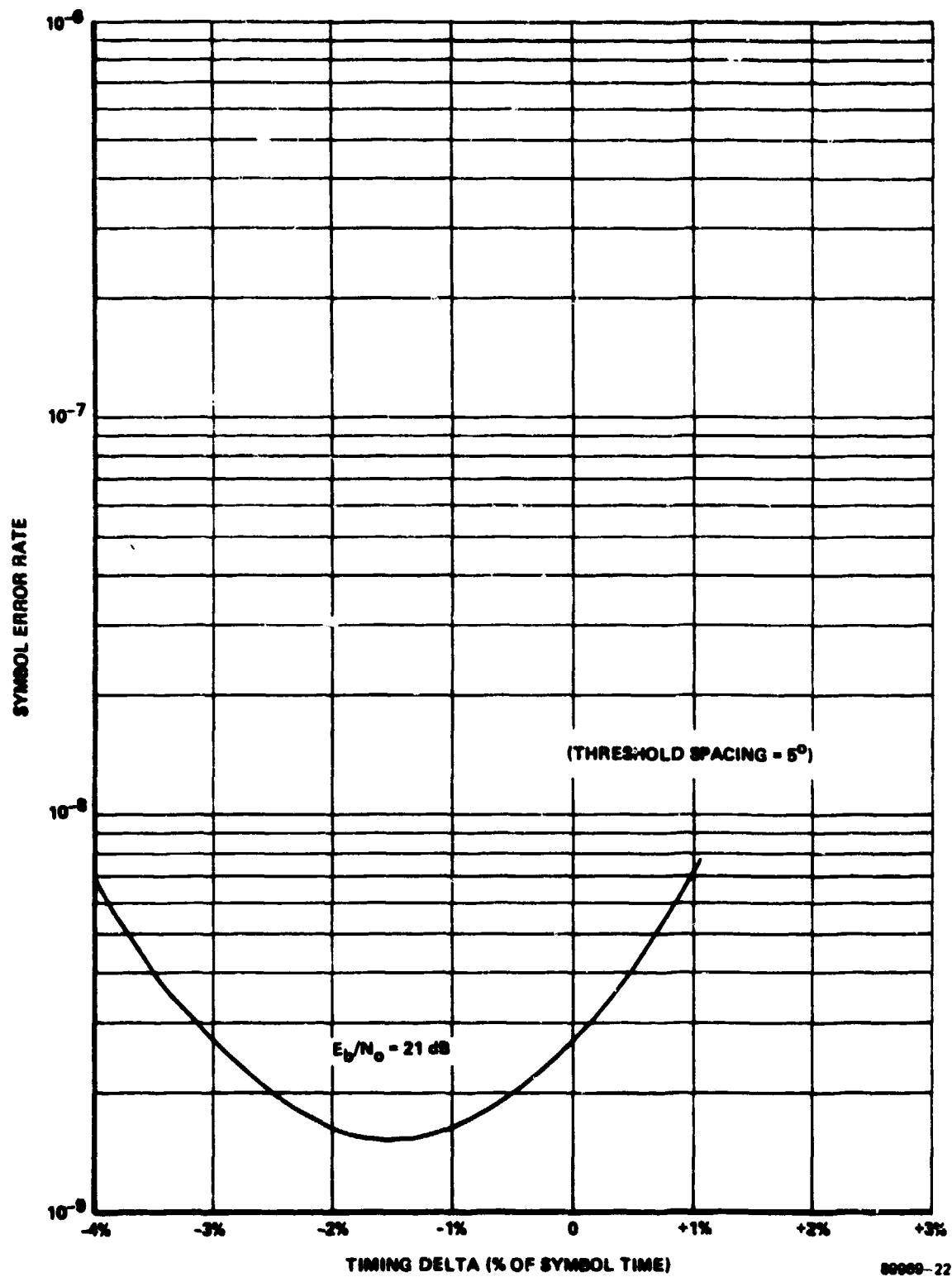
Figure 25. Nominal Waveguide Baseline Timing Sensitivity

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2.3.2.1 The Phase Detector Reference Problem

The original breadboard had some severe implementation problems which resulted in critical timing adjustments. The most severe problems arose from the technique employed to generate and use the coherent reference for the quadrature phase detector (QPD).

Figure 26 shows a basic conceptual block diagram of the prior breadboard demodulator. Conceptually, the demodulator functions as follows. A reference is established at the lowest of the four transmitted
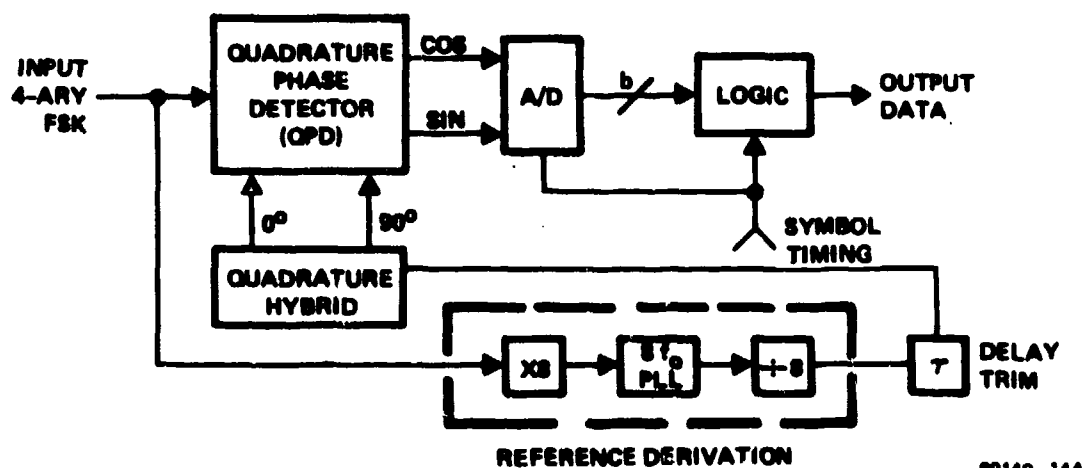
Figure 26. Simplified Diagram of Breadboard Phase Detection Technique

frequencies, f_0. This reference is used to provide phase measurements from the QPD. These phase measurements are quantized in the A/D converter and provided to digital logic which estimates the transmitted frequencies, taking into account any crosstalk generated by system filtering.

The phase detector reference loop in the breadboard operated open-loop from the phase measurements being derived with that reference which resulted in significant critical timing problems. In Figure 26, note that the reference is derived in a X8 frequency multiplier chain followed by a phase-locked loop (PLL). Because of inherent delays that arise in various paths of the circuit, a time delay trim, τ, is required to properly align the phase of the reference. If everything were ideal (in particular

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if time delays remained fixed) the system as shown would be satisfactory. However, with any variation leading to differential time delay between the QPD input and its reference, the reference is no longer coherent. It is believed that the intolerance of the previous breadboard to frequency offset could be traced to the fact that such offset resulted in changes in the differential time delay between the reference and QPD input. The following describes the steps taken to eliminate this problem in the present modem.

The possibility of making the QPD provide the error signal for controlling the phase of the reference VCO in a closed-loop manner as shown in Figure 27 has been investigated. As shown, the QPD outputs are observed and a phase measurement is noted. From this phase measurement a phase error to the closest FSK signal phase node can be calculated. For mod-index equal 1/8 FSK, the possible symbol-end phase nodes are spaced by 45°. The phase error signal so generated is filtered and used to control the VCO as shown.

An advantage of this type reference loop is that the reference is controlled to cause the phase error to the nearest node to average zero - where the phase error is based upon the actual phases measured in the QPD and not in an independently operating reference derivation loop. The coherence of the reference is thus guaranteed in a closed-loop manner.

During the study phase, attention was focussed on a scheme for deriving the phase error measurement described above from the existing phase detector thresholds in the demodulator. Figure 28 shows the manner in which the QPD quantizes the phase measurement for use in the logic processing circuitry. Ten thresholds are established on each of the two quadrature outputs. As shown in Figure 28 these thresholds allow 5 phase thresholds spaced by approximately 5° between each of the ideal ending phase nodes. Figure 29 shows a representative ideal phase node and the phase bins within $\pm 22.5^O$ of this node implied by the QPD thresholds of Figure 28.

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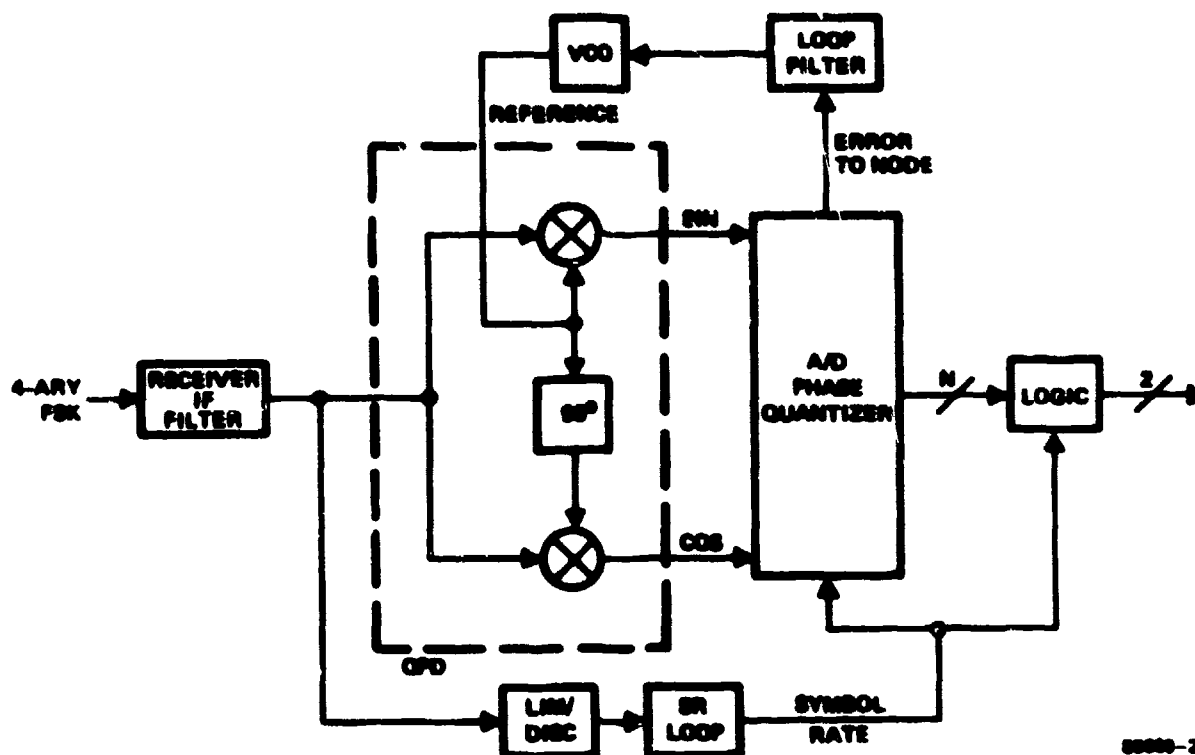
Figure 27. Closed Loop Reference Derivation

An error signal is derived from the existing slicing levels
wherein the phase error is assigned a value proportional to the distance of
the phase bin from the ideal node. Figure 29 shows that the 5 phase errors
associated with the 5 bins are $0, \pm15^{0}$, and $\pm20^{0}$. This is a rather
coarse quantization of the phase error.

Computer simulations were run to observe acquisition time,
loop-caused phase jitter, and symbol error rate obtainable with the scheme
which filters the coarse phase error signal to control the reference VCO.
Figure 30 shows the results obtained. The various quantities of interest
are plotted versus the natural frequency, ω_n, of the closed loop. The
loop damping factor was held constant at unity as the natural frequency was
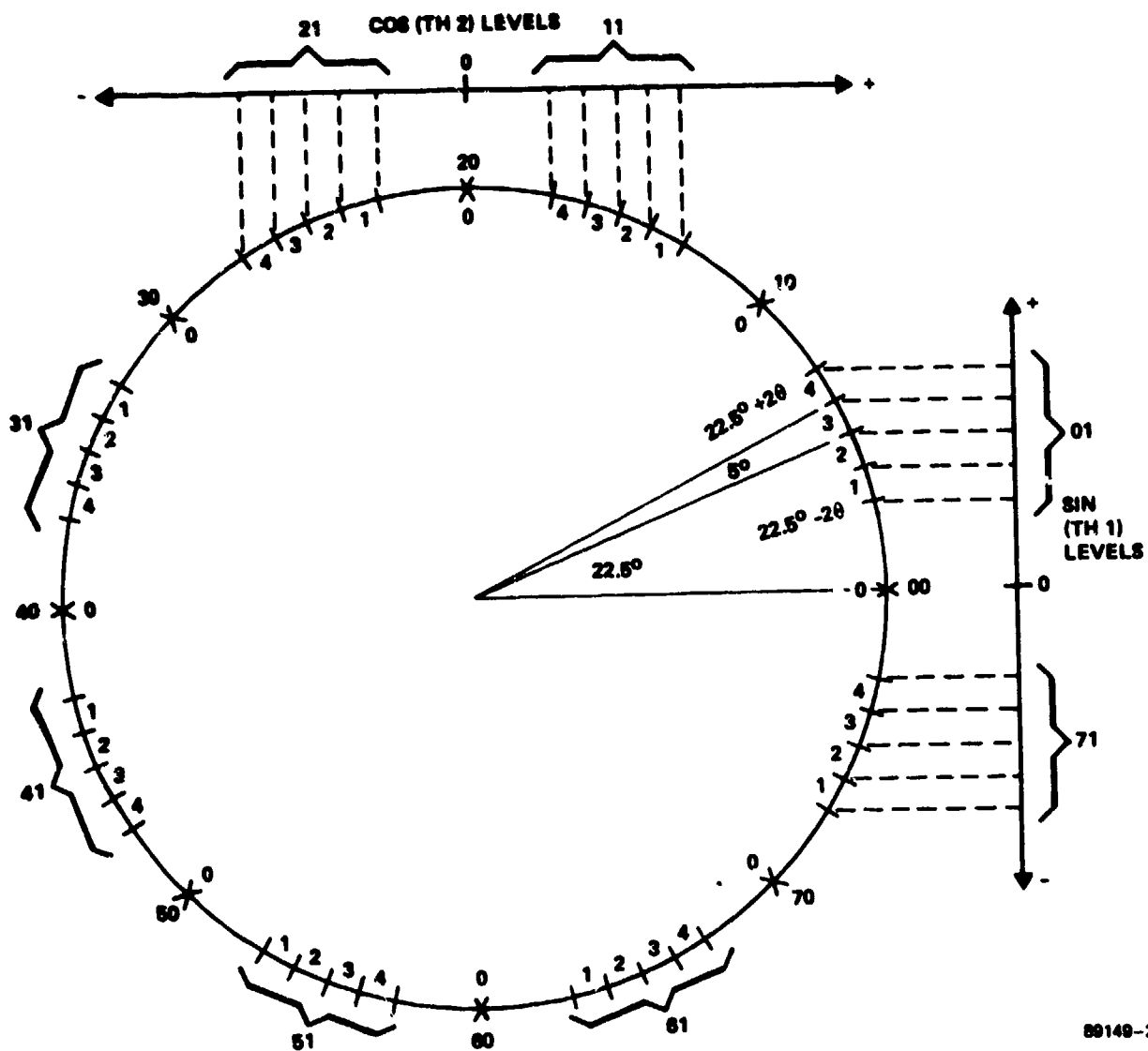
42

Figure 28. Threshold Settings

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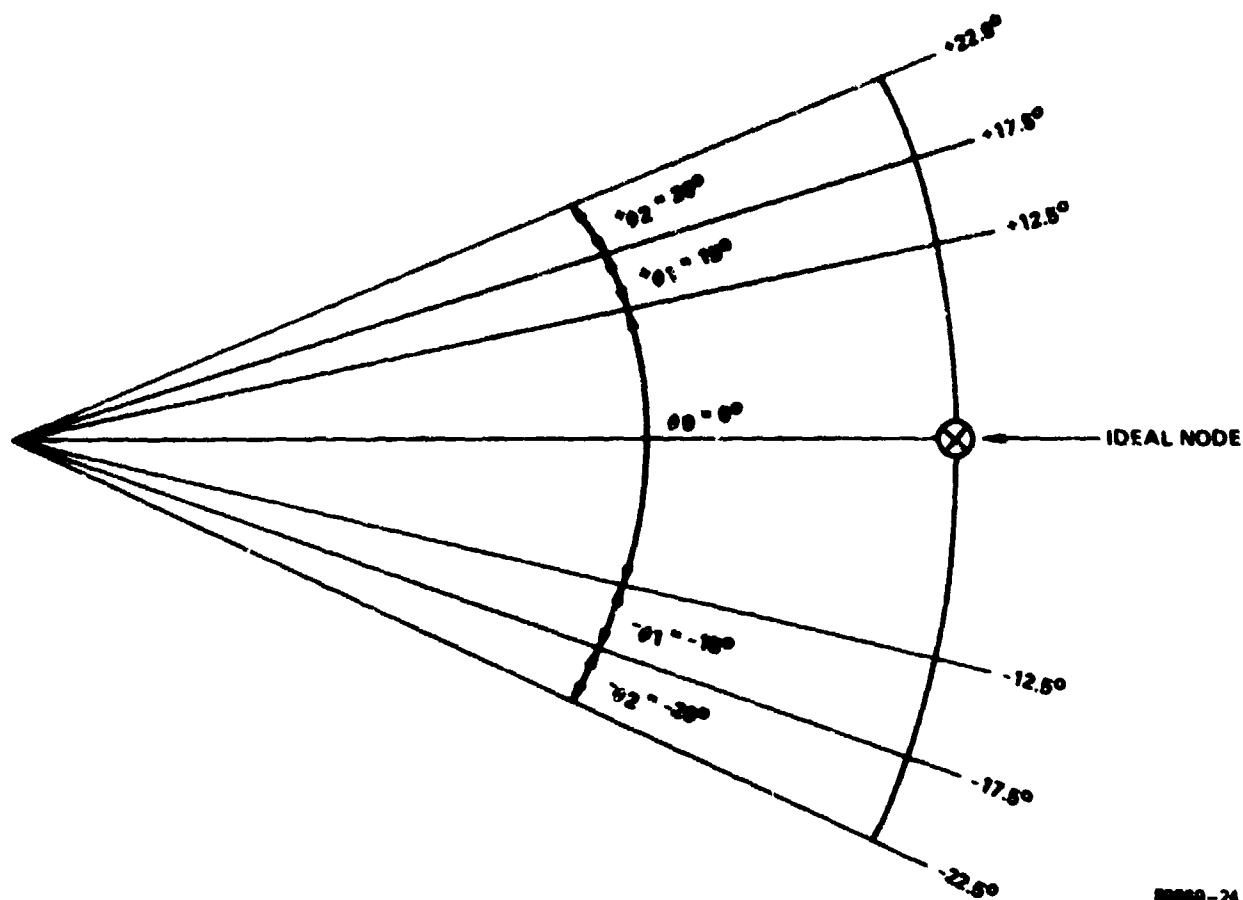
Figure 29. A Representative Ideal Node and Surrounding Phase Bins With the Thresholds of Figure 28

varied. The acquisition time varies rapidly with ω_n $(\sim\omega_n^{-3})$. The acquisition time plotted is for 80 kHz of initial frequency offset. E_b/N_o for all curves is 20 dB.

      To achieve the design goal of 1 ms acquisition time for 80 kHz offset, it is apparent from Figure 30 that the loop bandwidth will have to be set at a fairly large value (at least 70 to 80 kHz ω_n) and then after acquisition switch to a narrow bandwidth (ω_n approximately 10 kHz) to reduce rms loop-caused phase jitter to a desirable level of 0.7^C.

      The basic block diagram for the closed-loop reference derivation scheme demodulator is shown in Figure 31.

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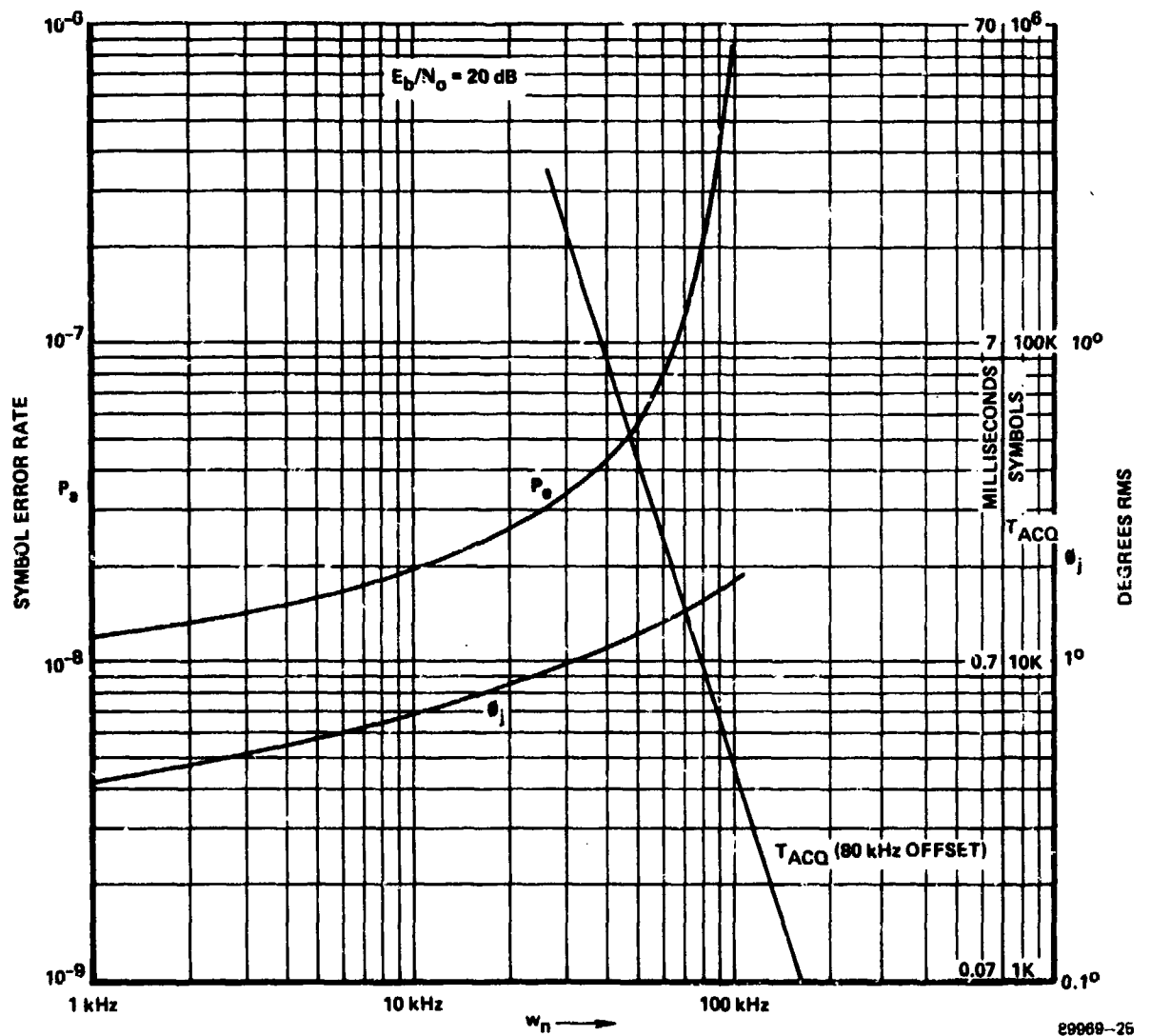
Figure 30. Closed Loop Phase Reference Scheme Characteristics
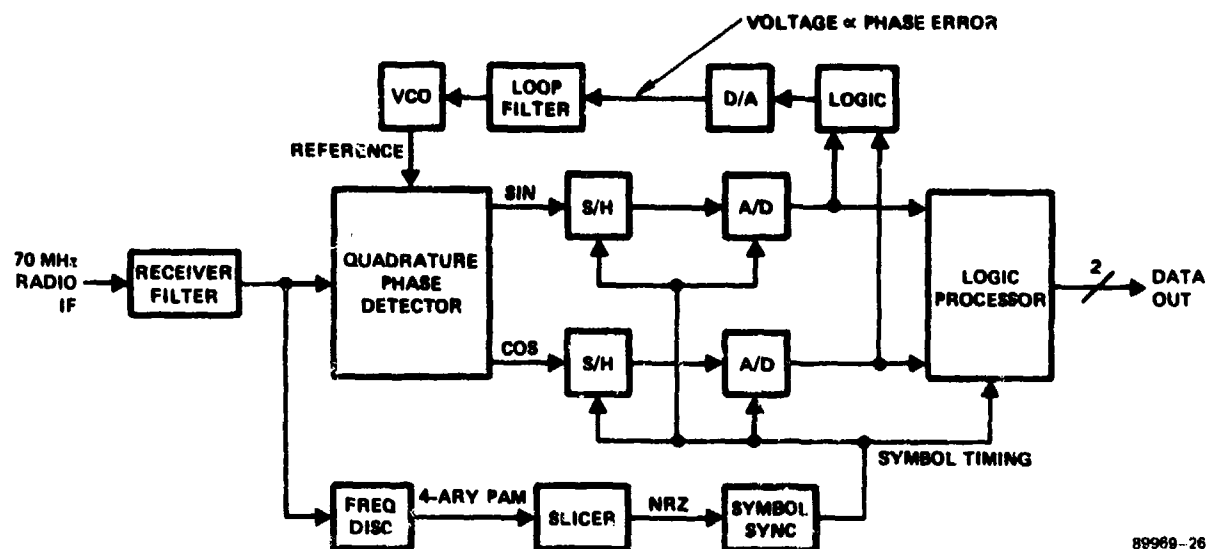
Figure 31.   Phase Detector - Demod for 4-ary CPFSK

The good results for the relatively simple closed loop scheme just described made the other more complex schemes that were considered look very unattractive and they were quickly discarded.

2.3.2.2   The Acquisition Problem

The primary acquisition problem occurs with the quadrature phase detector reference loop.   The original goal was 1 ms acquisition with 80 kHz of frequency offset.

With 80 kHz frequency offset, the closed-loop technique described above requires a loop bandwidth of approximately 100 kHz to acquire in 1 ms.   This loop bandwidth results in degradation due to excessive phase jitter of roughly two orders of magnitude in error rate. Thus, it is necessary to switch to a narrower loop following acquisition in order to reduce the jitter.   Simulation indicated that a loop bandwidth of

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approximately 10 kHz is required to reduce jitter to a desired level of 0.7° rms.

The provision of two different loop bandwidths is a complicating factor in the implementation. Not only are there special implementation problems brought on by the necessity to switch loop filters, but also the requirement for acquisition loop bandwidth of 100 kHz reflects into a requirement (from stability considerations) for a crystal VCO response bandwidth which stresses the capabilities of such VCO's.

It was desirable to eliminate the requirement to switch between two different loop bandwidths brought on by the 1 ms design goal. Several alternative approaches follow:

1. Increase the allowable acquisition time for 80 kHz frequency offset.

2. Reduce the frequency offset and keep 1 ms acquisition time.

3. Combination of reduced frequency offset and greater than 1 msec acquisition.

These three alternatives are summarized in Table 3. These numbers are generated from the computer simulation shown in Figure 30 and assuming that acquisition behavior is as in a second order phase-locked loop (which our closed-loop scheme is), i.e., $T_{acq} \propto (\Delta f)^2 \, \omega_n^{-3}$ where Δf is frequency offset and ω_n = loop natural frequency.

Frequency stability of 10^{-7} would hold frequency offset to under 1 kHz at 8 GHz and such stability would allow one loop bandwidth acquisition in 1 ms and no baseline degradation.

In consultation with RADC an assumption of 20 kHz frequency offset and 20 ms goal on acquisition was adopted. A single loop bandwidth of 14 kHz which as indicated by the bottom line in Table 3 results in no more than 0.1 dB baseline degradation was implemented.

Table 3. Effect of Changing Acquisition Specification on the Single Loop BW Reference Scheme

	Freq. Offset (kHz)	Acq. Time (MS)	Loop Nat. Freq. (kHz)	Baseline Degradation (dB)
Alternative 1	80	4	50	0.5
	80	7	40	0.3
	80	18	30	0.25
	80	32	25	0.2
	80	60	20	0.1
	80	320	14	0.1
Alternative 2	40	1	63	0.6
	30	1	52	0.5
	20	1	40	0.3
	10	1	25	0.2
Alternative 3	40	32	20	0.15
	30	32	16	0.1
	20	32	13	~ 0
	10	32	8	0
	20	20	14	~0.1

2.3.2.3 Dual B/Hz Capability

A relatively simple technique was uncovered during the study phase for providing 1 B/Hz as well as 2 B/Hz capability in the modem. The technique exploits maximal equipment commonality between the two modes of operation in both modulator and demodulator. The technique allows 13.41 Mb/s operation in the 1 B/Hz mode and 26.82 Mb/s operation in the 2 B/Hz mode - both operating in an authorized bandwidth of 14 MHz.

The approach involves using mod-index 1/4 4-ary FSK in the 1 B/Hz mode and mod-index 1/8 4-ary FSK in the 2 B/Hz mode. At the modulator, operation as described above results in both modes utilizing the same four modulation frequencies. The 1 B/Hz mode simply selects one of the four synthesized frequencies at one-half the rate (6.705 MHz) as the 2 B/Hz mode (13.41 MHz). Thus, the modulator is common between the two modes.

Figure 32 shows the manner in which the two modes are handled at the demodulator. In the 2 B/Hz mode the 70 MHz radio IF signal is filtered by a 13.41 MHz (symbol rate) 3 dB bandwidth filter and passed directly on to
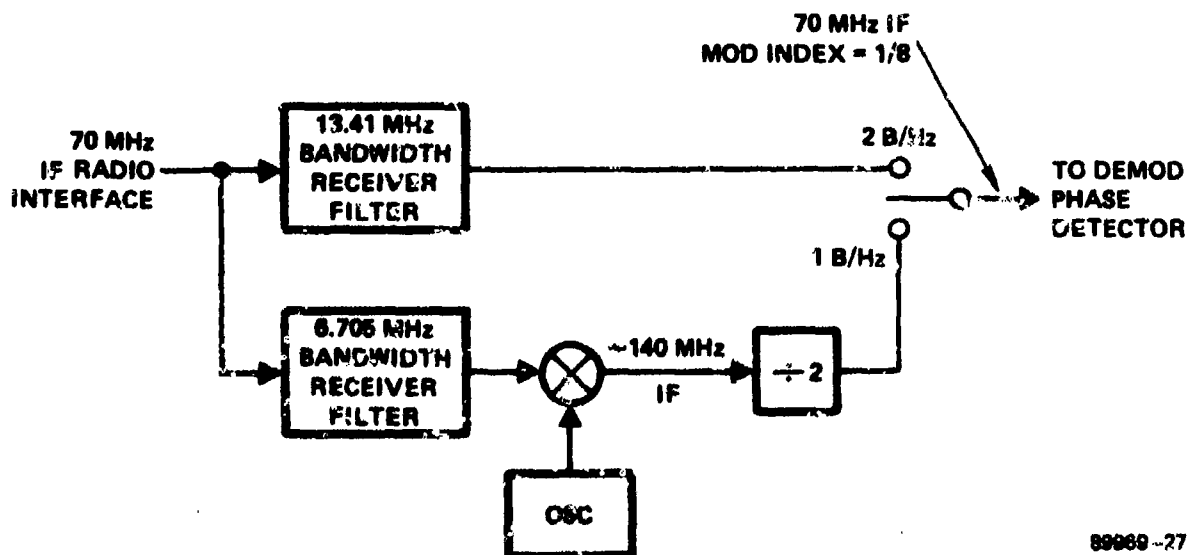
Figure 32. Dual B/Hz Conversion Demodulator Front-End

the demodulator phase detector and A/D which is designed under the assumption of mod-index 1/8 4-ary FSK input (the ideal phase nodes are spaced by 45°). In the 1 B/Hz mode on the other hand a conversion step is included as shown to convert the received mod-index 1/4 signal to mod-index 1/8 after ltering by a 6.705 MHz (again, symbol rate for this mode) 3 dB bandw dth IF filter. This conversion is accomplished by first mixing to a nominal 140 MHz IF frequency followed by frequency divide-by-2 to produce a nominal 70 MHz mod-index 1/8 IF signal which once again is appropriate to feed to the phase detector and A/D for further processing. Fortunately, the signal phase distortion produced by the 6.705 MHz bandwidth filter in the 1 B/Hz mode is almost exactly twice that in the 2 B/Hz mode. As a result, after the frequency divide-by-2 operation (+2 counter) the signal phase distortion is identical between the two modes. Further, this means that the phase quantizing thresholds in the phase detector are identical between the two modes. Thus, the only differences in the demodulator required between the modes are the changes required to handle the two different symbol rates (reference loop bandwidth change and symbol timing loop change).

The approximate 6 dB improvement in performance of the 1 B/Hz mode over the 2 B/Hz mode can be thought of in light of this conversion step in the following way. The ideal phase node spacing of the converted signals are identical (45°) for the two modes. Because of the divide-by-2 operation in the 1 B/Hz mode, however, the rms noise-caused phase jitter is halved. This is the source of the 6 dB improved performance.

2.3.2.4   New Receiver IF Filter

During this study it was found that a 4-pole Butterworth filter with two sections of all-pass phase compensation performed better than the prior modem's 4-pole Bessel filter. The 3 dB bandwidth is equal to the 4-ary symbol rate. The attenuation and group delay distortion characteristics of this filter are shown in Figure 33.

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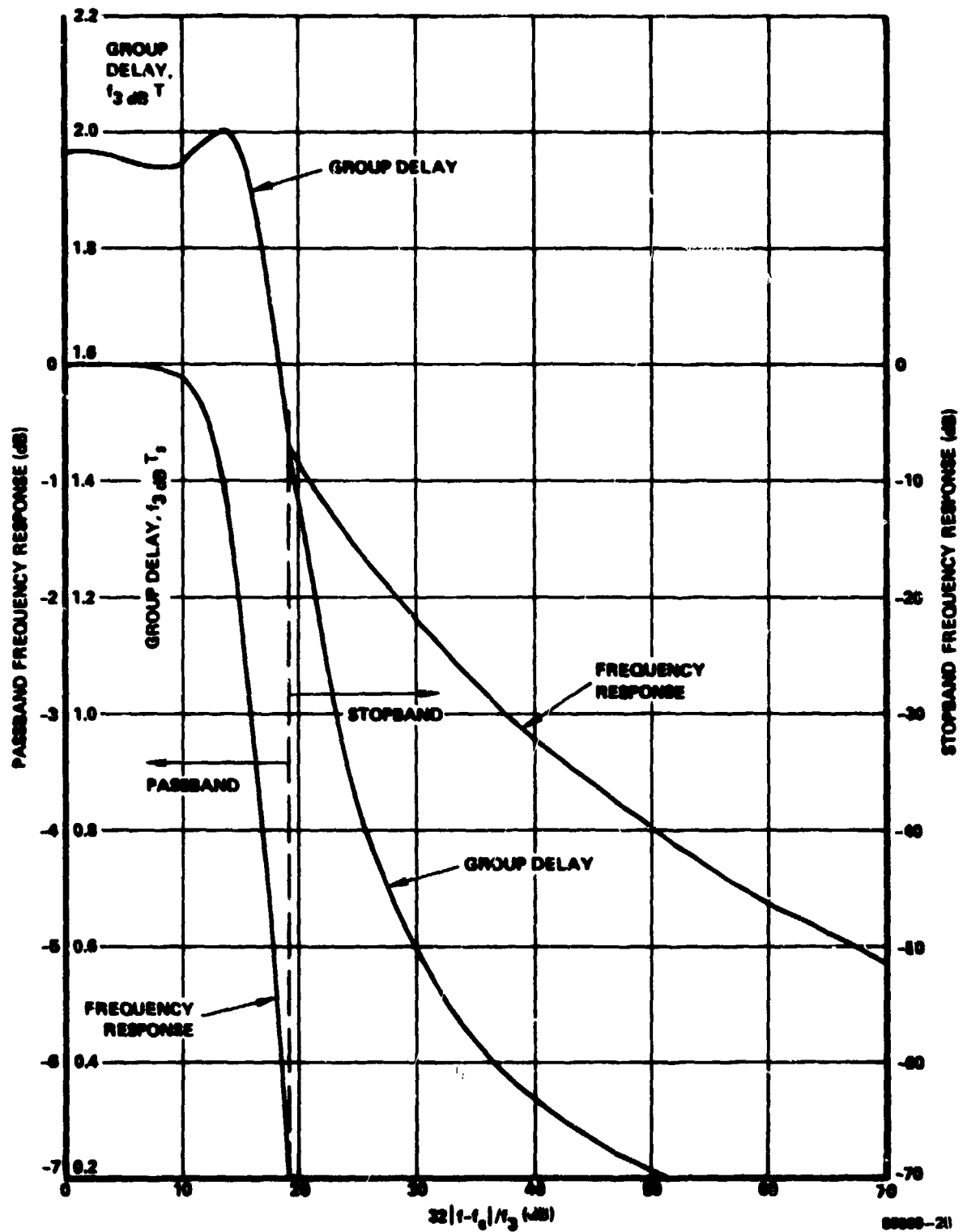
Figure 33. RCVR Filter Characteristics

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SECTION 3.0

HARDWARE DESCRIPTION

3.0   HARDWARE DESCRIPTION

An experimental modem incorporating the baseline concepts described in Section 2.0 was constructed. The actual hardware is described in this section. The modulator and demodulator sections of the modem are physically packaged separately.

3.1   Modulator

The modulator is contained in a 5.25 inch high chassis designed to be mounted in a standard 19-inch rack. The unit contains integral power supplies and cooling fan. It should be noted that as cooling air is drawn into the chassis from the top, a minimum space of 3.5 inches is required above the unit.

A photograph of the modulator front panel is shown in Figure 34. Input data is applied to jacks A and B.
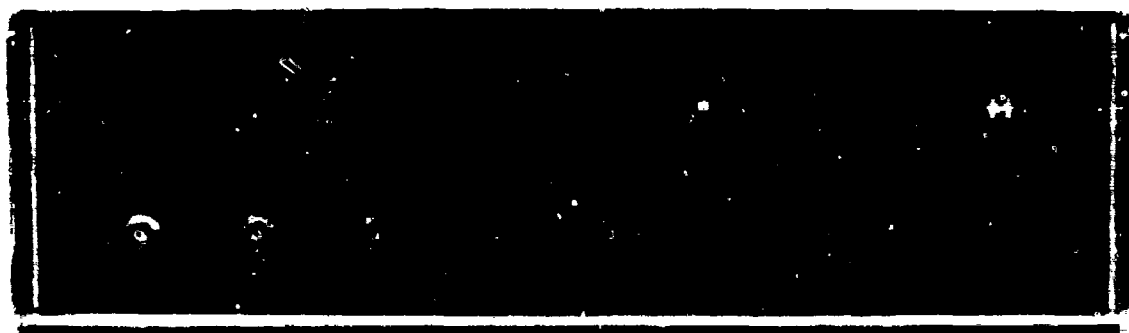
Figure 34.   Modulator Front Panel

For 2 B/Hz, 26.82 Mb/s single stream operation and 1 B/Hz, 13.41 Mb/s single stream operation, channel A is used exclusively. For 2 B/Hz and two synchronous 13.41 Mb/s stream operation, channels A and B are multiplexed together within the modulator producing a single internal 26.82 Mb/s data stream. An input bit rate clock, synchronous with the input data must be applied to the INPUT CLOCK jack. The data transition should occur on the rising edge of the clock. Exact alignment is not required, but

timing should be within 1/4 bit time. A transmit clock is provided at the OUTPUT CLOCK jack. Its frequency is crystal-controlled and automatically switches from 26.82 MHz to 13.41 MHz as required when the MODE switch is operated. The three most counterclockwise positions of the MODE switch are for 2 B/Hz operation. Position A is for use with a single 26.82 Mb/s data stream (applied to jack A). Position A+B is for multiplexing two 13.41 Mb/s data streams together (jacks A and B). The position labeled TEST reconfigures the internal 20-stage randomizer for use as a pseudorandom sequence generator. No external data or clocks need be applied in this mode. The two most clockwise positions of the MODE switch are used for 1 B/Hz operation. Position A is for a single 13.41 Mb/s input data stream (jack A). There are no multiplexing provisions in the 1 B/Hz mode. The 1 B/Hz TEST position allows for internal generation of a 13.41 Mb/s pseudorandom data stream. The IF OUTPUT jack provides a modulated 70 MHz signal at a nominal level of +1 dBm.

All front panel jacks are BNC type and are designed to interface with 75 ohm circuits. Digital input and output levels are nominally 2 volts peak-to-peak with +1 volt being a "1" and -1 volt a "0".

A conceptual block diagram of the Modulator is shown in Figure 35. Its theory of operation is identical to that of the previous modem where pairs of data bits are used to select one of four phase coherent frequencies each symbol time. The four tones are generated by mixing an 8 times bit rate clock with bit rate and symbol rate. This forms a mod-index 1 signal which is divided by 8 to generate the desired mod-index 1/8 signal which is mixed up to 70 MHz. The primary difference between this modulator and the previous one is the phase-locked loop (PLL) that locks to the externally supplied bit rate clock. This PLL supplies all the modulator clocks, including the 8 times bit rate clock used in the frequency generator. Thus, the four tones have a fixed time relationship to the symbol rate clock that selects the desired tone.

Input data is applied to lines A and B. For 2 B/Hz single stream operation and 1 B/Hz operation, channel A is used exclusively. For 2 B/Hz and two synchronous 13.41 Mb/s stream operation, channels A and B are fed to the MUX where a single 26.82 Mb/s stream is produced. This

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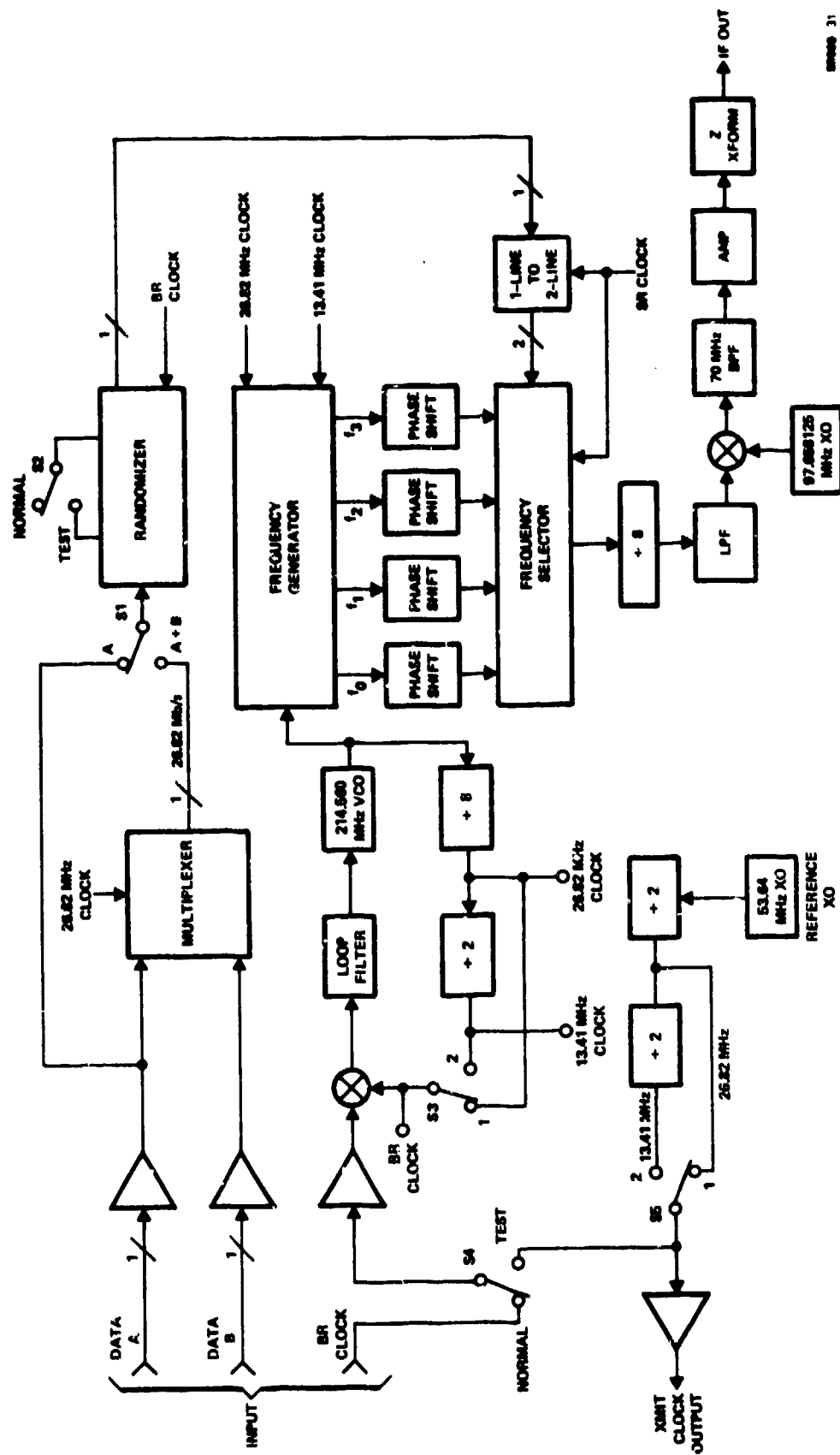
Figure 35. Modulator Block Diagram

stream is randomized and fed to the Frequency Selector. In the test mode, the randomizer is used to produce a pseudorandom sequence and requires only a clock input. For this mode, the clock PLL locks to an internal reference clock which also supplies a transmit clock to the outside world.

One B/Hz operation is provided by selecting the tones (which remain the same) at one half the 2 B/Hz symbol rate, producing a mod-index 1/4 signal.

3.2   Demodulator

The demodulator is contained in an 8.75-inch high chassis designed to fit a standard 19-inch rack. The unit contains integral power supplies and cooling fan. As cooling air is drawn into the top of the chassis, a minimum space of 3.5 inches above the unit is required.

A photograph of the demodulator front panel is shown in Figure 36. The demodulator receives IF at 70 MHz, +1 dBm at the IF IN jack.

Figure 36.   Demodulator Front Panel

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Input impedance is 75 ohms. Output data appears at jacks A and B. Recovered bit rate timing appears at the CLOCK OUTPUT jack. The data transitions occur on the rising edge of this clock. In the self-test mode (selected at the modulator) bit errors detected by the internal self-synchronizing derandomizer produce positive pulses on the BIT ERROR OUTPUT jack. Normally, this output remains at a logic "0" (-1.0 V into 75 ohms) when the modem is operating error-free in the TEST mode. All logic outputs provide 2 volts peak-to-peak into a 75 ohm load. A logic "1" is represented by +1.0 volt and a logic "0" by -1.0 volt.

The MODE switch has three positions. The two most counterclockwise positions select 2 B/Hz operation. Position A is used when the modulator receives a single 26.82 Mb/s data stream. This position is also used for the 2 B/Hz TEST mode (selected at the modulator). Position A+B corresponds to the similarly marked position on the modulator when the data input consists of two synchronous 13.41 Mb/s data streams. The single 1 B/Hz position, A, is used for both 13.41 Mb/s data stream operation and the 1 B/Hz TEST mode. With the demodulator MODE switch set to the position corresponding to that chosen on the modulator, the output data appearing at jacks A and B corresponds to the input data at the input jacks on the modulator bearing the same label.

With the modulator in one of the two TEST modes, the data outputs on the demodulator will remain at a logic "1" when the modem is operating error-free. The BIT ERROR OUTPUT produces a half-bit period pulse for each error detected. Bit error rate performance can be determined by measuring the frequency at the BIT ERROR OUTPUT jack and dividing this number by the bit rate (26.82 Mb/s or 13.41 Mb/s). The derandomizer is of such a design that it will produce three pulses for every isolated error made by the processing logic. This corresponds to normal operation when the randomizer/derandomizer introduces an approximate factor of three degradation in bit error rate performance.

A conceptual block diagram of the Demodulator is shown in Figure 37. In 2 B/Hz mode, the 70 MHz IF is fed to a linear phase, matched filter and then to a limiter. In 1 B/Hz operation, the mod-index 1/4 signal is fed to another matched filter and is then mixed up to approximately twice
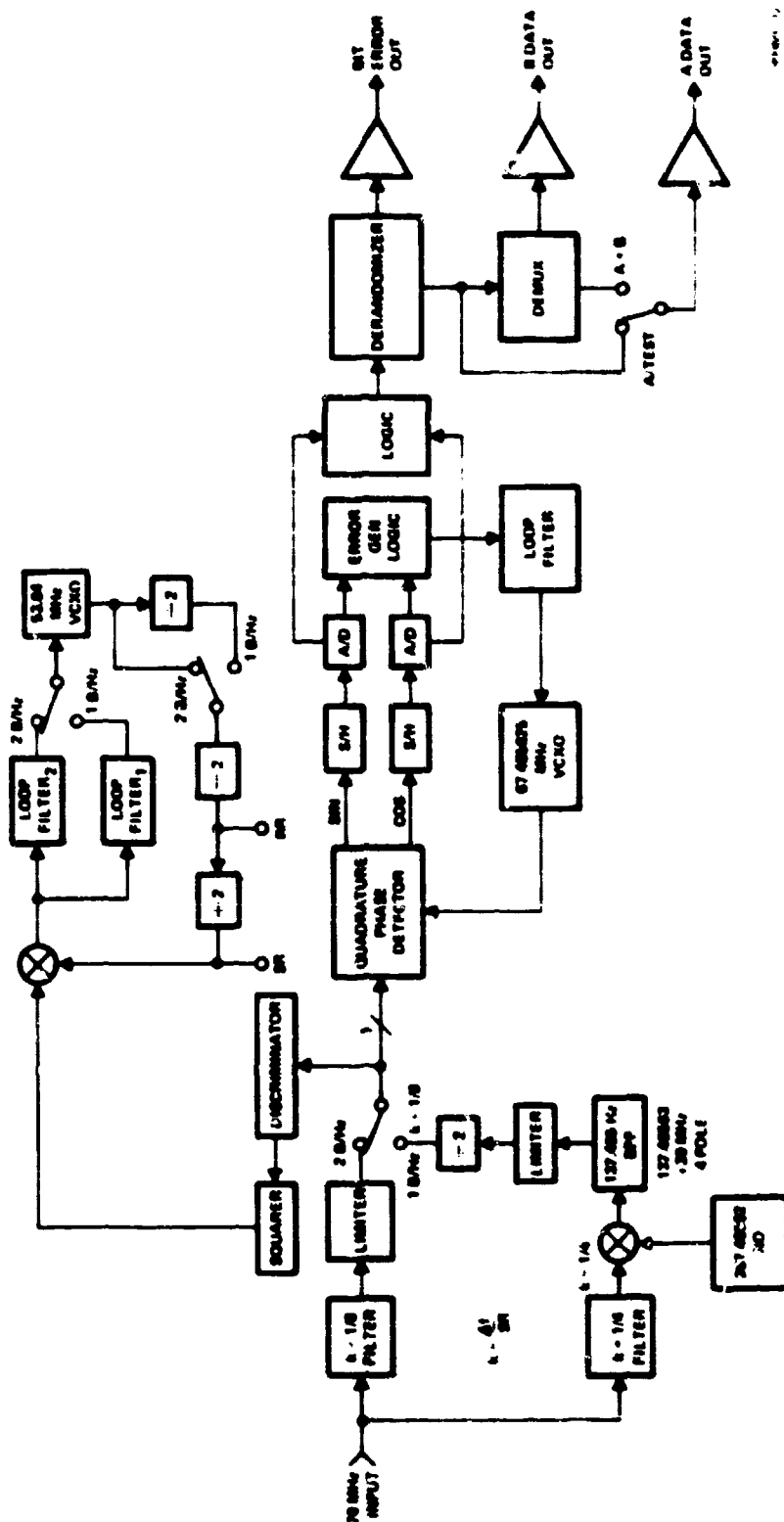
Figure 37. Demodulator Block Diagram

the center frequency and then divided by two to produce a mod-index 1/8 signal. It is then processed the same as the 2 B/Hz signal.

The limited signal is applied to the quadrature phase detector. The phase measurements of the sine and cosine channels are sampled and held while their values are digitized by the A/D's. Logic circuitry is used to derive an error signal from the phase measurements. This error signal is used to drive a VCXO through the loop filter. The VCXO provides the reference for the phase detector. The loop closure thus aligns the reference to minimize the average error to the phase modes. The A/D outputs also go to the processing logic. This logic is identical in concept to that used in the breadboard developed on the previous contract (F30602-74-C-0263). For a detailed explanation of its operation, refer to Final Technical Report RADC-TR-76-117. The recovered data from the logic goes to the self-synchronizing derandomizer. The derandomized data is fed to the demux which can be bypassed for single stream operation.

Demod timing is recovered by a discriminator on the limited input signal producing a PAM sequence. Squaring recovers the symbol rate component to which a PLL is locked, providing symbol rate and bit rate clocks for the demodulator.

3.3   FCC 19311 Waveguide Filter

In order to meet the spectral requirements of FCC Docket 19311, a microwave filtering approach was used. The filter is a waveguide section designed to be installed directly into the LC8D radio, replacing the final transmitter output filter.

The desired filter characteristics were specified as follows:

Electrical Characteristic Desired:

1) Attenuation and group delay characteristics associated with a 4-pole Butterworth filter. (See Figures 15 through 18 for detail)

2) 3 dB bandwidth = 16 MHz

3) Center frequency at room temperature (25° C) = 8.075 GHz

4) Detuning versus temperature: Center frequency shift < $\pm$450 kHz over 0° to 50° C temperature

5) Insertion loss: < 1 dB

6) Max. VSWR: 1.1

7) Critical attenuations required: At room temperature (25° C) at 8.075 GHz $\pm$13.41 MHz filter must be 19 dB down

Mechanical Characteristics

1. Waveguide size: WR112

2. Dimensional information:

   a) Flange-to-flange: 7" in-line

   b) Max., dimension at right angle: 4" (oneside only)

3. Flange type: UG-51 for WR112 waveguide

The filter was manufactured by MDL. The specifications were treated as design goals. The filter delivered to Harris ESD failed to meet the desired group delay distortion characteristics. The actual filter's group delay distortion is shown in Figure 38. The excessive group delay peaks near the band edges account for much of the excess degradation introduced by the filter. It was determined that group delay compensation introduced at IF should be investigated during the test program at RADC.
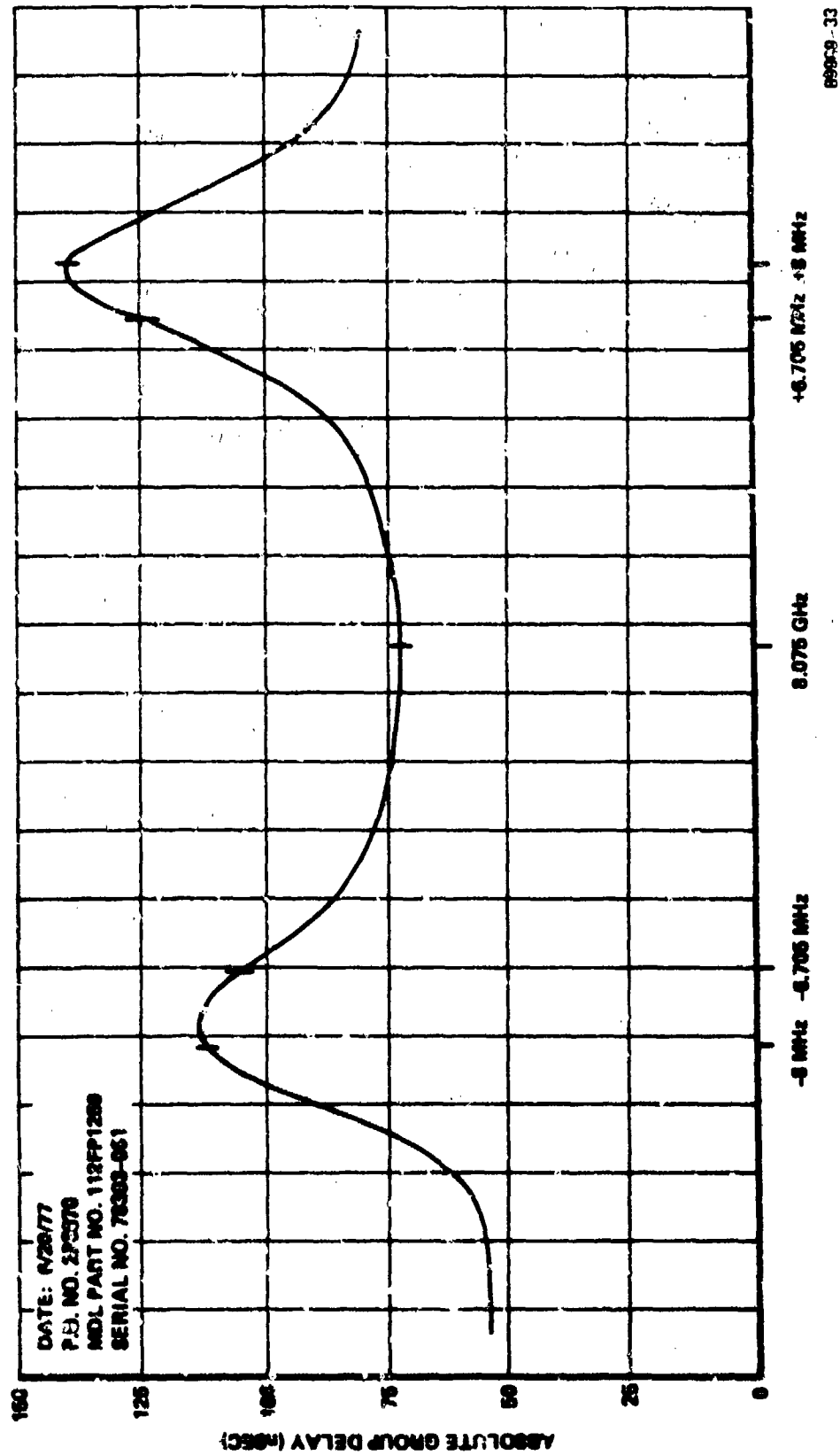
Figure 38. Group Delay Distortion 4-Pole Butterworth Waveguide Filter

SECTION 4.0

TEST RESULTS

4.0   TEST RESULTS

The test program was performed at Harris ESD in Melbourne, Florida, and at RADC in Rome, New York. The in-plant tests were designed to provide a performance baseline from which to interpret results from later radio tests and to verify the characteristics of various internal parameters. These tests were performed with the modem looped back at 70 MHz with additive thermal noise. Tests were also performed with the modem looped back through an up/downconverter allowing the introduction of the FCC 19311 waveguide filter to the signal path. The RADC tests included back-to-back tests at 70 MHz and tests through the LC8D radio connected back-to-back. The test plan which describes test setups and procedures is included in this report as Appendix C.

In this section, the test results are presented. Modem performance was very good and all design requirements were met. In addition the modem performance came very close to meeting all design objectives.

4.1   In-Plant Tests

This paragraph presents data acquired at Harris ESD during the period of November 1, 1977 through November 4, 1977.

4.1.1   Spectral Efficiency Results

Since the actual spectrum presented at the radio transmitter output is the true measure of compliance with FCC Docket 19311, tests performed at Harris ESD could only be useful as preliminary indicators. Hence, detailed plots were taken only at RADC. However, photographs were taken at Harris ESD of the spectra at 70 MHz at the Modulator output and at the output of the up/down converter that contained the FCC 19311 waveguide filter. Figure 39 shows the 2 B/Hz spectrum directly at the modulator output. Figure 40 shows the 2 B/Hz spectrum after the waveguide filter and down-conversion to 70 MHz. Examination of these spectra indicated that the
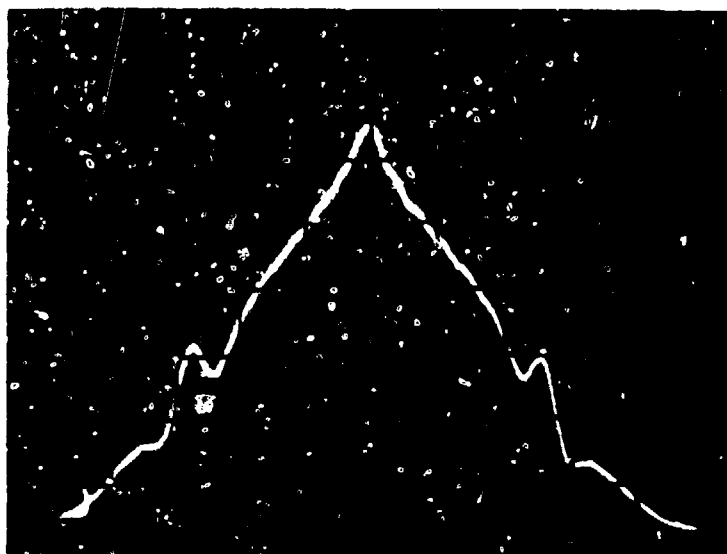
BIF   = 300 kHz

B_V = 100 Hz

VERTICAL - 10 dB/DIV
                0 dB = TOTAL
                        POWER

HORIZONTAL - 5 MHz/DIV

11/1/77

Figure 39.   2 B/Hz Spectrum Without FCC 19311 Filter
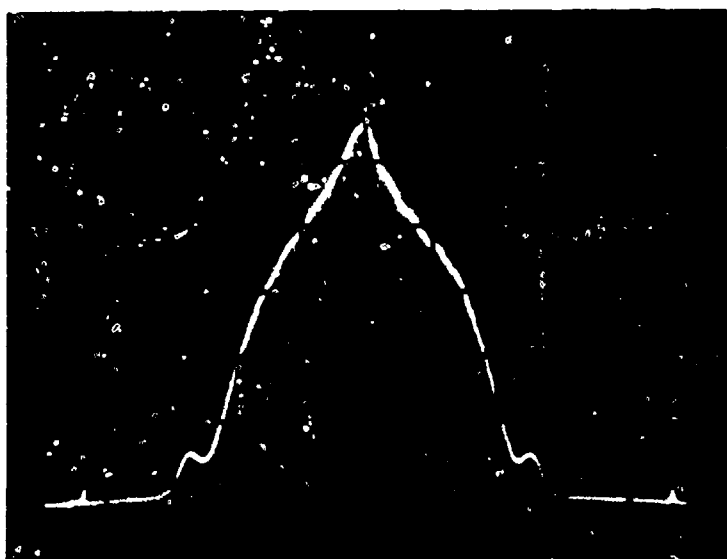
BIF = 300 kHz

B_V = 100 Hz

VERTICAL - 10 dB/DIV
                0 dB = TOTAL
                        POWER

HORIZONTAL - 5 MHz/D'V

11/1/77

Figure 40.   2 B/Hz Spectrum With FCC 19311 Filter

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filter performed as expected and that the requirements of FCC 19311 would be met.

The 1 B/Hz spectrum before and after filtering is shown in Figures 41 and 42 respectively. Compliance with FCC Docket 19311 was also indicated here.
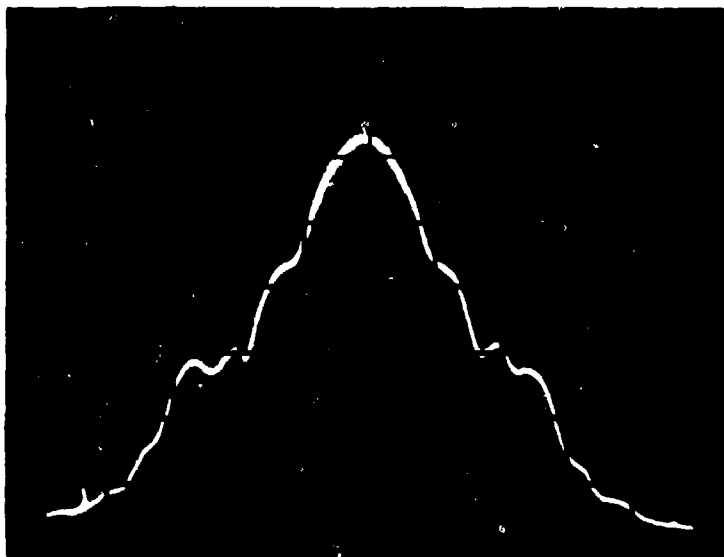
BIF = 300 kHz

B_V = 100 Hz

VERTICAL - 10 dB/DIV
        0 dB = TOTAL
                POWER

HORIZONTAL - 5 MHz/DIV

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Figure 41.   1 B/Hz Spectrum Without FCC 19311 Filter
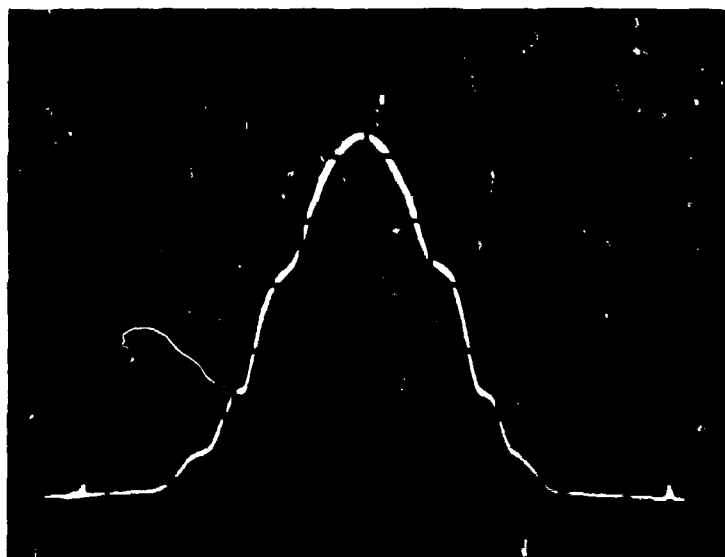
BIF = 300 kHz

B_V = 100 Hz

VERTICAL - 10 dB/DIV
        0 dB = TOTAL
                POWER

HORIZONTAL - 5 MHz/DIV

11/1/77

Figure 42.   1 B/Hz Spectrum With FCC 19311 Filter

More detailed and documented spectral results are presented in the RADC test result section.

4.1.2 BER Vs E_b/N_o

The design objective for the modem was a bit error rate of 5×10^{-9} or less at an E_b/N_o of 22 dB when operating through the Philco Ford LC8D radio for a nominal 2 B/Hz spectral efficiency. The design objective for a nominal 1 B/Hz spectral efficiency under the same conditions was 5×10^{-9} bit error rate at an E_b/N_o of 16 dB. These design goals are for performance without the 20 stage randomizer/ derandomizer, which was not to degrade BER by more than a factor of 3 in the vicinity of a 1×10^{-7} BER. The BER was measured in a variety of configurations, as described below. Details of the test configuration and calibration are in Appendix C.

4.1.2.1 2 B/Hz Test Results

To obtain baseline performance data, the modulator and demodulator were connected directly at 70 MHz. Thermal noise with an equivalent bandwidth of 41.5 MHz was added at 70 MHz. Initially, the internal randomizer/derandomizer was bypassed and the plot shown in Figure 43 was obtained with an external data generator and error counter. The measured data is shown with a computer baseline prediction described in Section 2.0. In the vicinity of a 5×10^{-9} BER, the measured data is approximately 0.8 dB from that predicted. At higher bit error rates, the difference is closer to 0.5 dB. A BER of 5×10^{-9} was obtained at an E_b/N_o of 20.6 dB back-to-back without randomizer.

Figure 44 shows 2 B/Hz back-to-back performance through the randomizer on Channel A with a single 26.82 Mb/s data stream. Comparison with Figure 43 shows that the randomizer introduced a BER degradation of less than a factor of three at any BER. Note that the computer-predicted curve has been shifted by a factor of three for all plots showing incorporation of the randomizer.
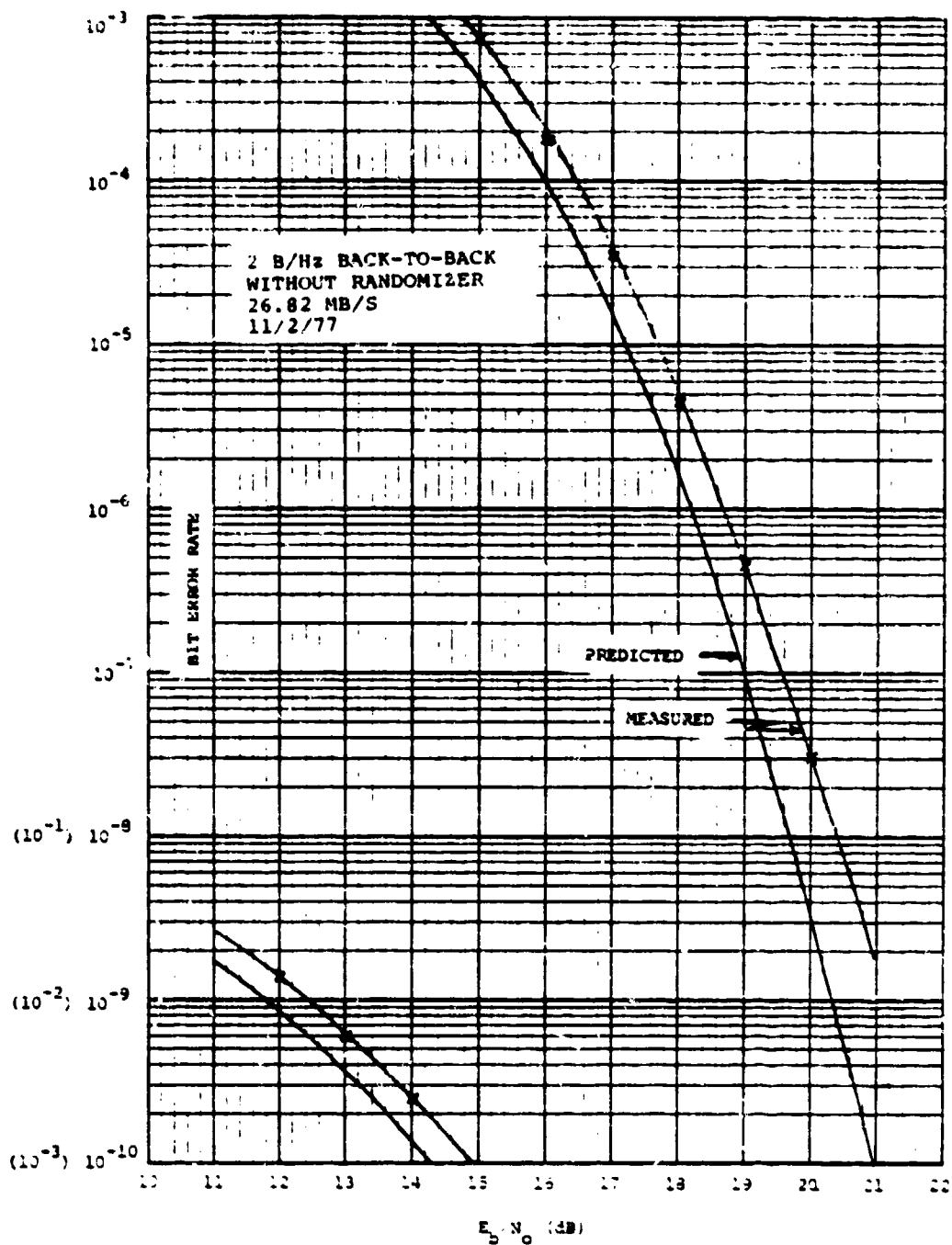
Figure 43. BER-2 B/Hz, Back-to-Back, Without Randomizer

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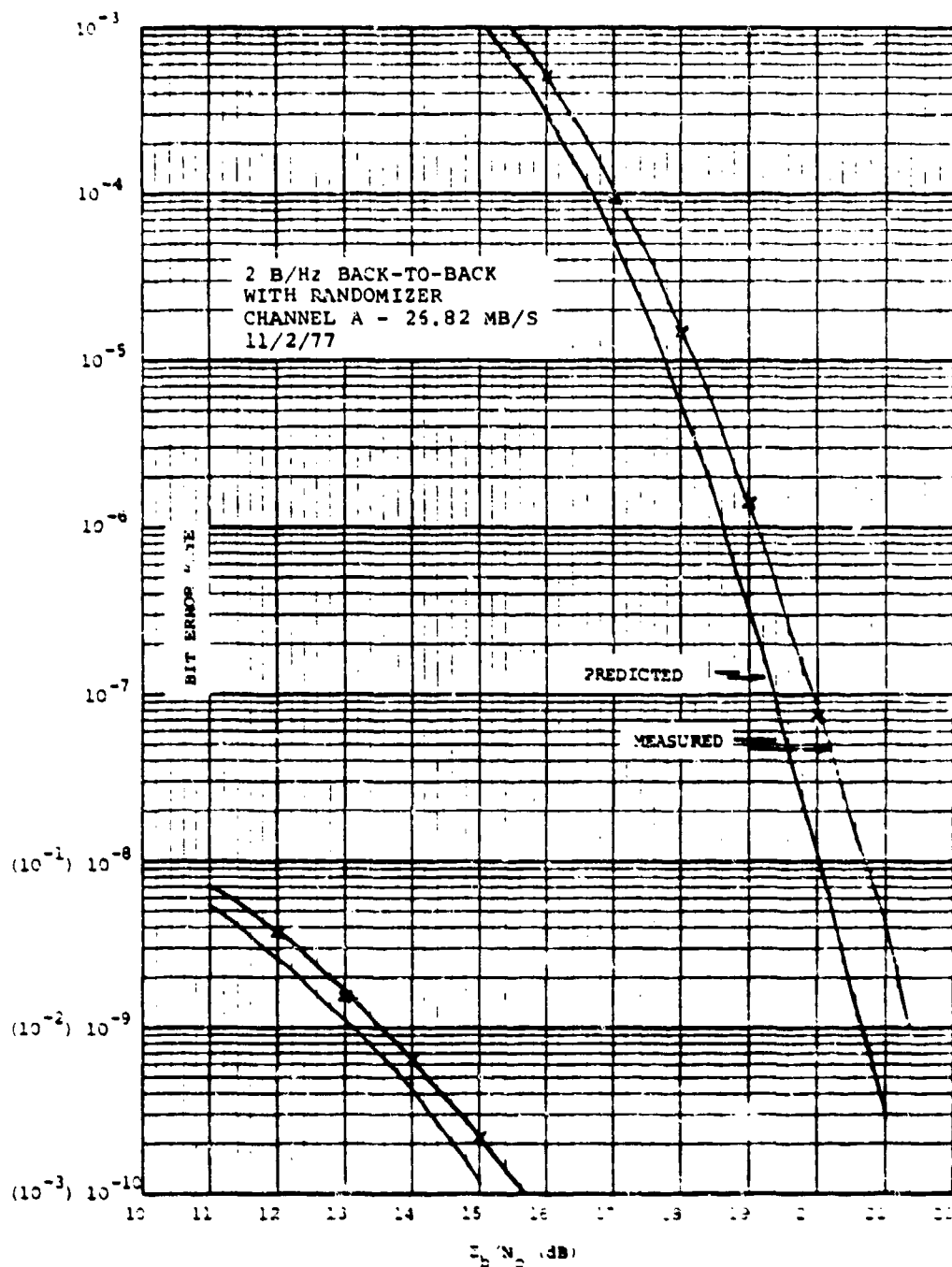
Figure 44.   BER-2 B/Hz, Back-to-Back, With Randomizer
Channel A - 26.82 Mb/s

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Figure 45 and Figure 46 demonstrate that performance in the A and B mode, where two synchronous 13.41 Mb/s data streams are multiplexed together, is essentially the same as that of the single 26.82 Mb/s data stream mode. Figure 47 shows performance as measured in the TEST MODE without benefit of external data generator and error detector. The resulting curve is virtually identical to that of Figure 44, demonstrating the validity of this test technique.

To simulate performance over the LC8D radio with FCC 19311 waveguide filter, the modulator output was upconverted to 8.075 GHz, filtered, and downconverted to 70 MHz where broadband noise was added. The results are shown in Figure 48. The randomizer was bypassed for this test to facilitate measurement. A BER of 5×10^{-9} was achieved at an E_b/N_o of 22.9 dB. This is about 2.3 dB from the prediction and about 0.9 dB from the design goal. These results indicated that group delay compensation at 70 MHz might be desirable with the LC8D radio.

4.1.2.2   1 B/Hz Test Results

Figure 49 shows the basic 1 B/Hz BER performance without randomizer. A BER of 5×10^{-9} was achieved at an E_b/N_o of 15.3 dB, which is approximately 1.3 dB from the predicted value. The same test run with randomizer resulted in a BER of 5×10^{-9} at an E_b/N_o of 15.7 dB. This curve is shown in Figure 50. As with 2 B/Hz operation, performance is degraded by no more than a factor of three by the randomizer. BER performance was also measured using the internal TEST MODE. Results are within measurement error of those obtained with external BER measurement equipment. A plot of this data may be found in Figure 51.

The use of the FCC 19311 waveguide filter has much less effect on 1 B/Hz operation than 2 B/Hz operation. This is a result of the more compact 1 B/Hz spectrum. Figure 52 depicts 1 B/Hz BER performance without randomizer. A BER of 5×10^{-9} occurred at an E_b/N_o of 15.6 dB. This exceeds the design goal by 0.4 dB. The computer simulation was 1.6 dB inside the measured value.
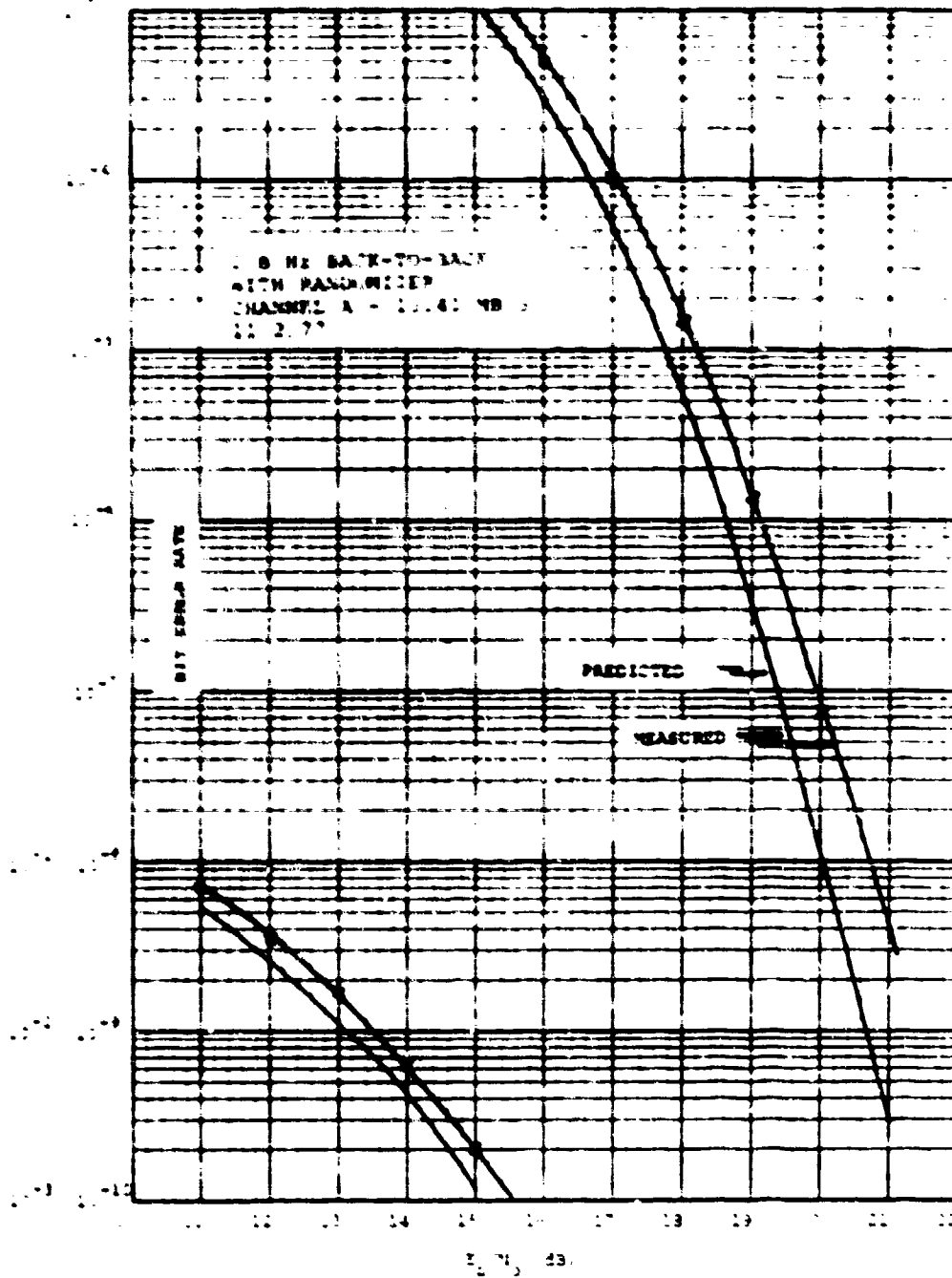
Figure 45.   BER-2 B/Hz, Back-to-Back, With Randomizer
Channel A - 13.41 Mb/s

71
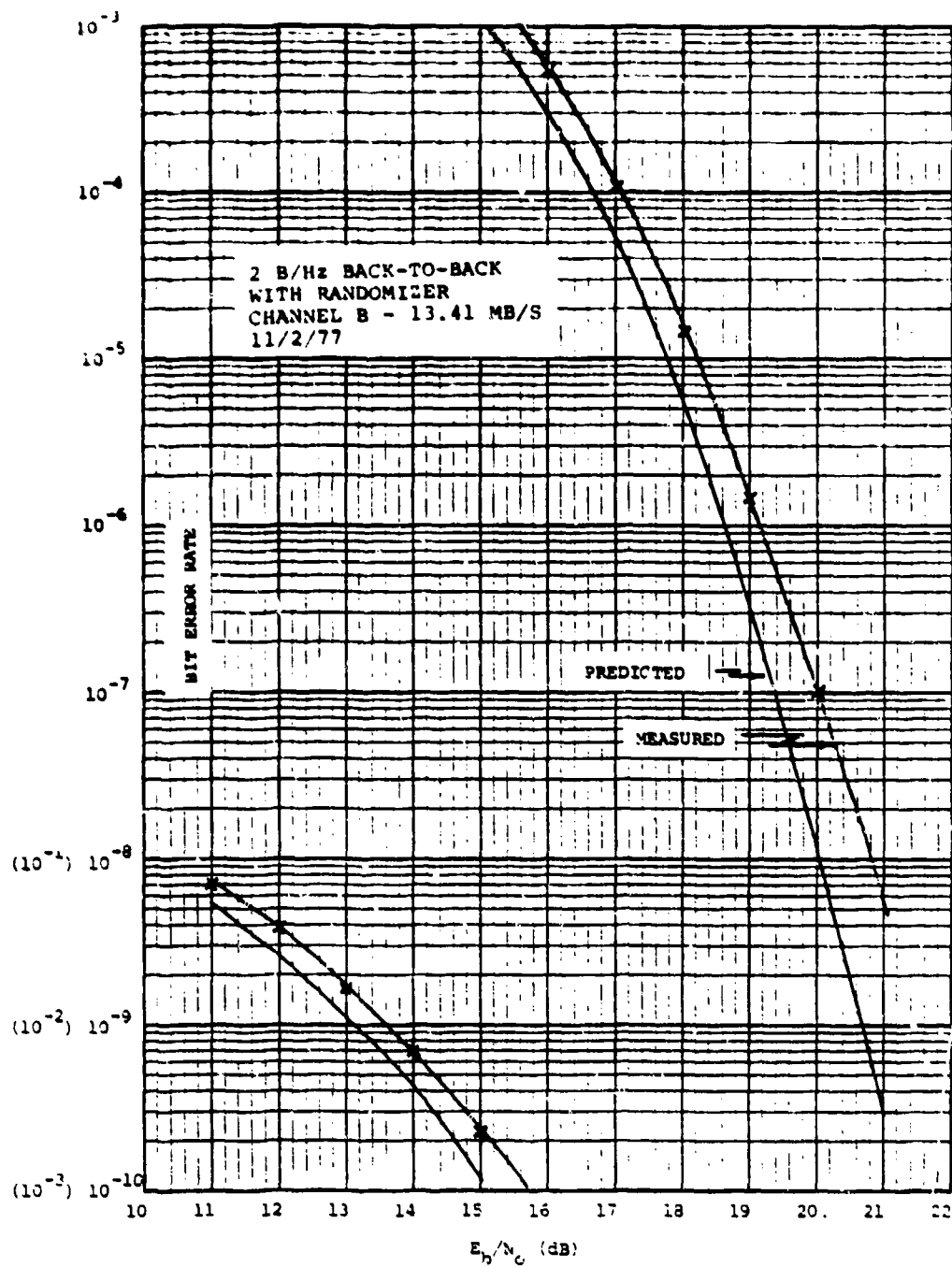
Figure 46. BER-2 B/Hz, Back-to-Back, With Randomizer
Channel B - 13.41 Mb/s
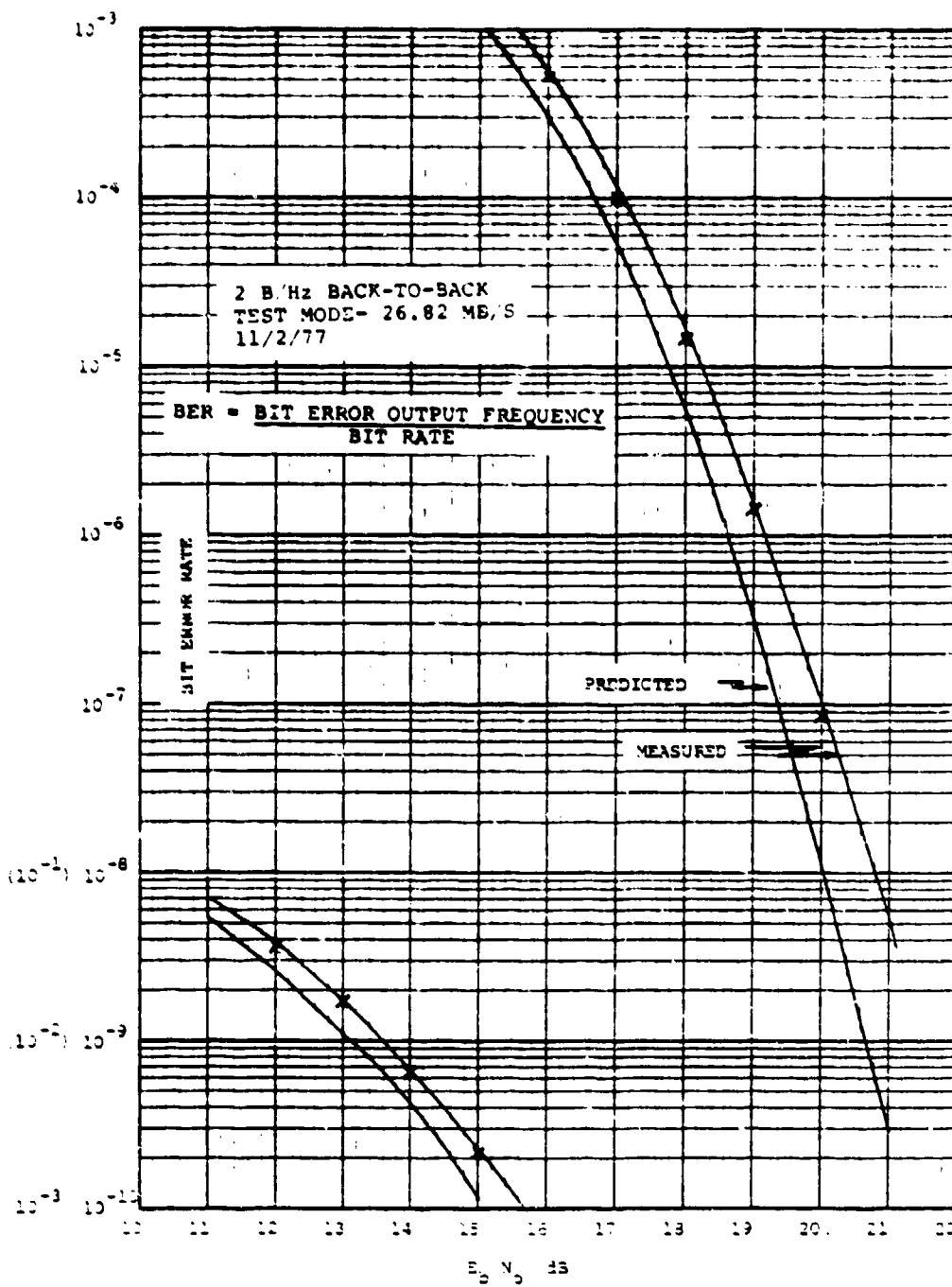
Figure 47. BER-2 B/Hz, Back-to-Back, Test Mode

73
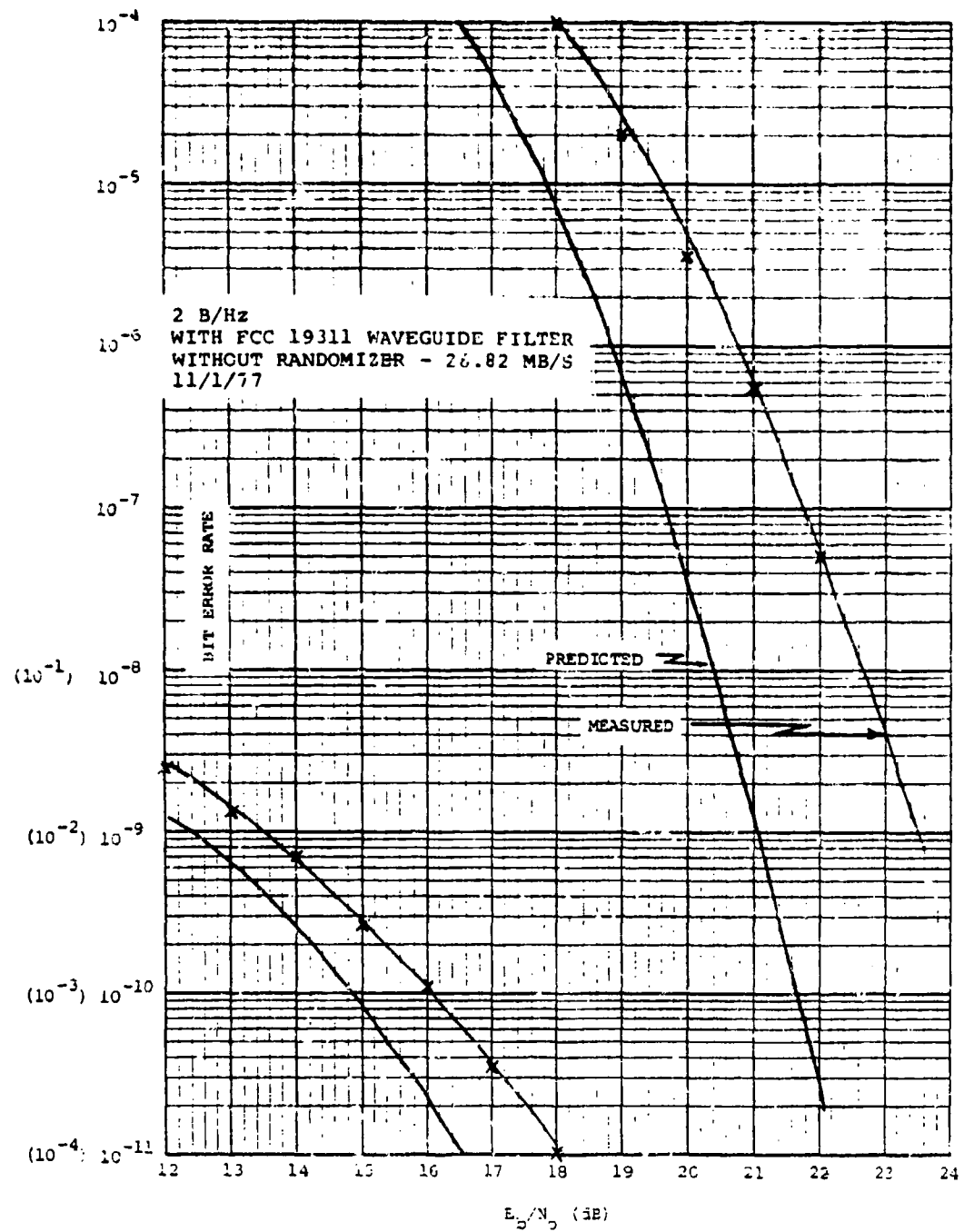
Figure 48. BER-2 B/Hz, With FCC 19311 Waveguide Filter, Without Randomizer

74
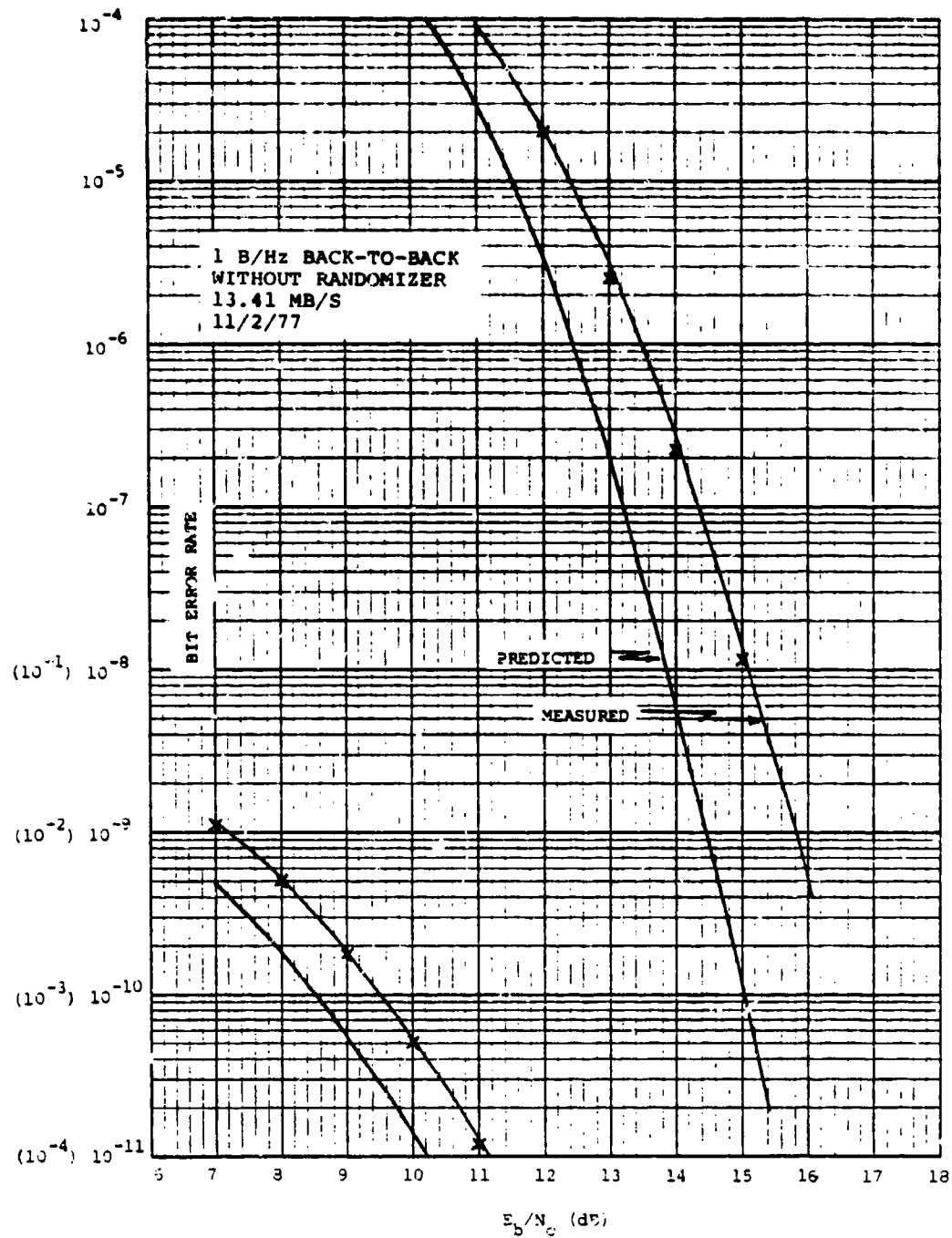
Figure 49. BER-1 B/Hz, Back-to-Back, Without Randomizer

75
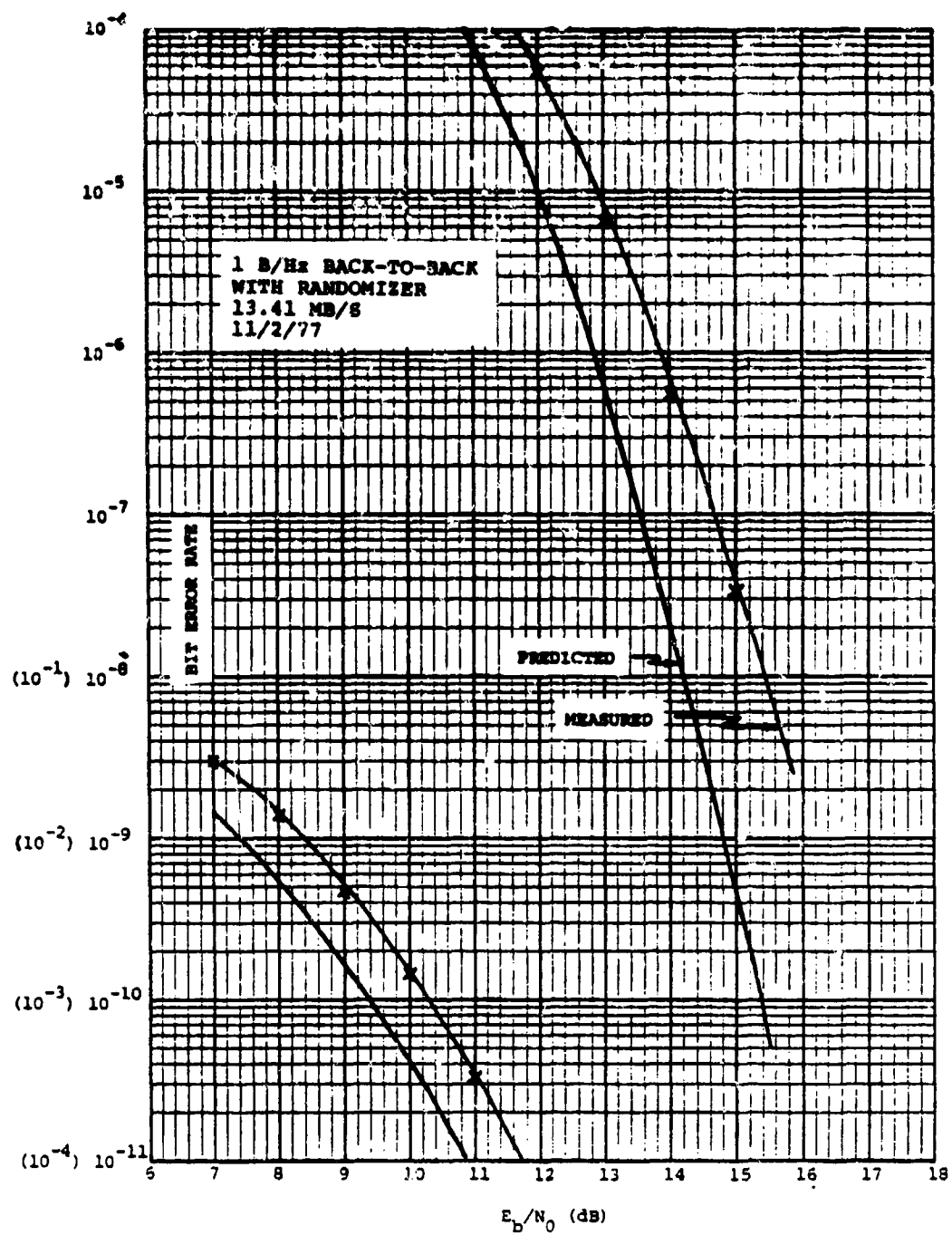
Figure 50. BER-1 B/Hz, Back-to-Back, With Randomizer
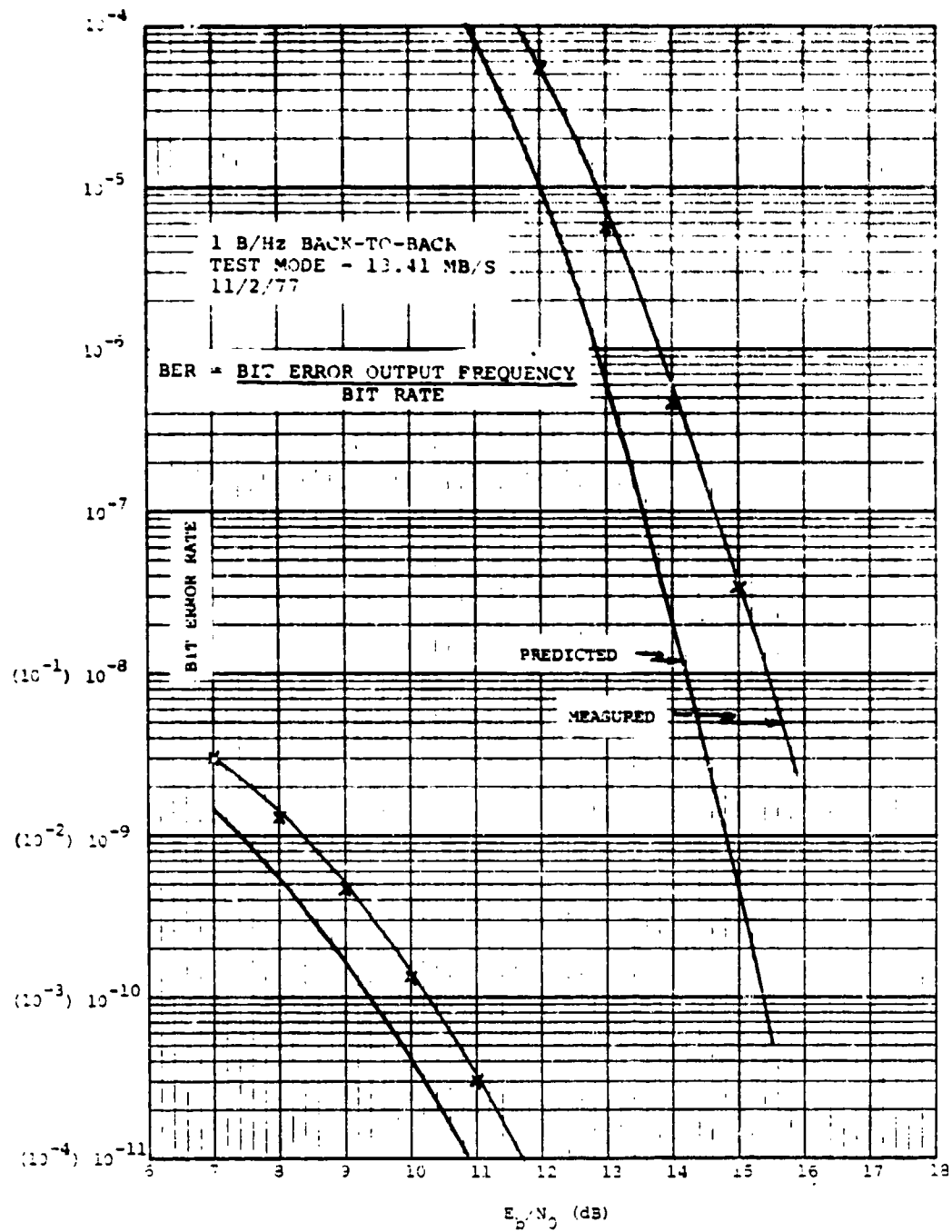
Figure 51. BER-1 B/Hz, Back-to-Back, Test Mode

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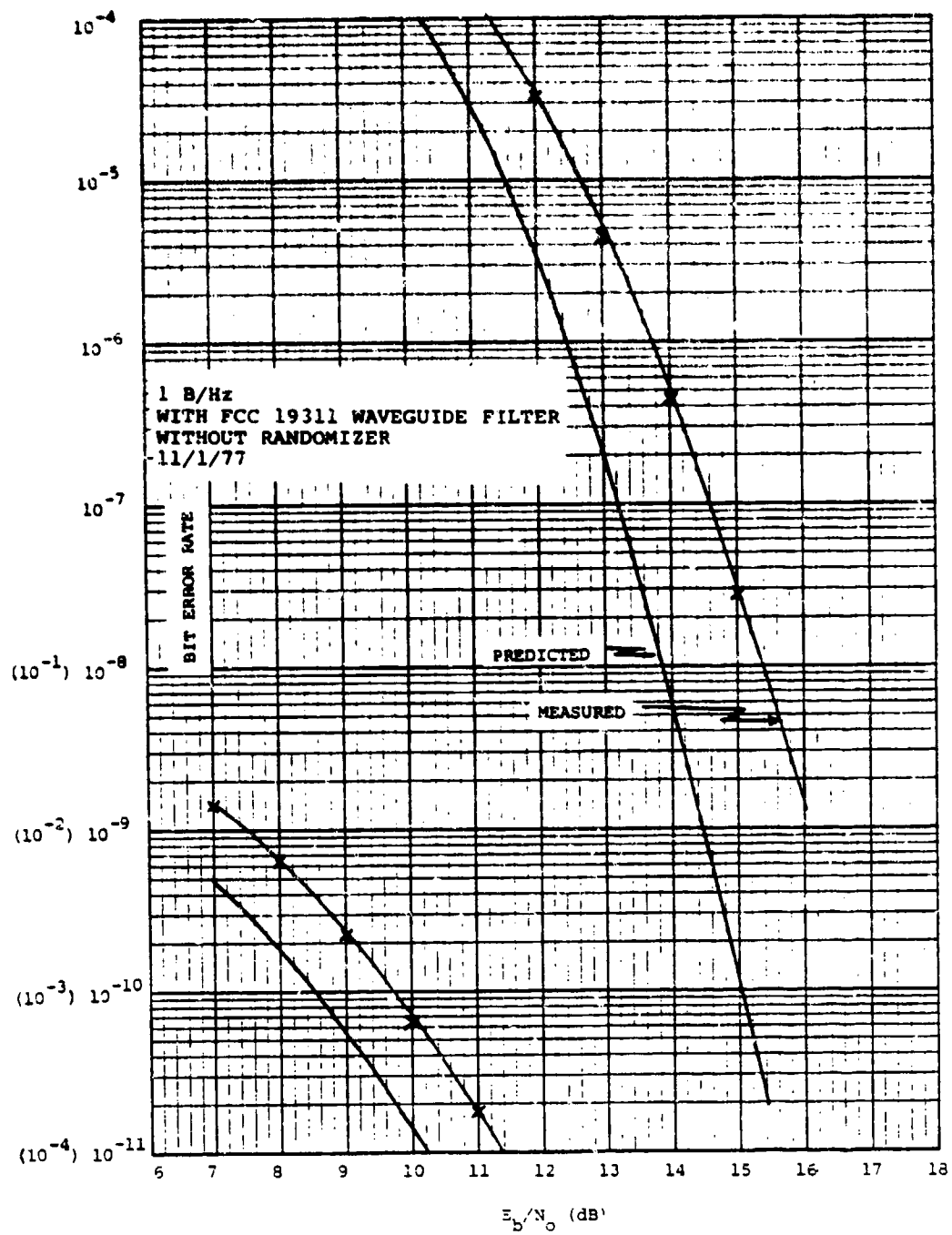
Figure 52. BER-1 B/Hz, With FCC 19311 Filter, Without Randomizer

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4.1.3 Acquisition Test Results

Acquisition performance was tested by gating the IF signal on and off with an electronic switch. The modem was run in the self-test mode and the BIT ERROR OUTPUT observed on an oscilloscope. Noise was added to the IF to produce a BER in the vicinity of 1×10^{-7} with the demodulator locked up. With the IF gated off, a 50 per cent error rate produces a large number of transitions of the BIT ERROR OUTPUT. When the IF is reapplied and acquisition achieved, the error rate is so low as to make transitions unobservable on the oscilloscope. The transition from high error rate to low may be observed on the scope and compared to the time at which the IF is gated on. The photograph in Figure 53 was exposed long enough to record about 10 acquisition attempts. The modem was operating in the 2 B/Hz mode with an IF offset of +20 kHz. The upper trace marks the application of IF to the demodulator with a positive transition. The error transitions on the lower trace cease in less than 10 ms, indicating acquisition. Long term observation revealed that more than 90 percent of all acquisition attempts were completed in less than 10 ms and none were observed to require more than 20 ms. The design goal was 20 ms with an offset of 20 kHz. The same results were obtained for an offset of -20 kHz (Figure 54).

Acquisition in 1 B/Hz mode was measured with the same test set-up. Sample acquisitions are shown in Figure 55 and Figure 56 for +20 kHz offsets and -20 kHz offsets respectively. Acquisition was achieved successfully in less than 15 ms in more than 90 percent of all trials. On rare occasions (judged to be less than 1 percent of all trials) 25 ms was required for acquisition.
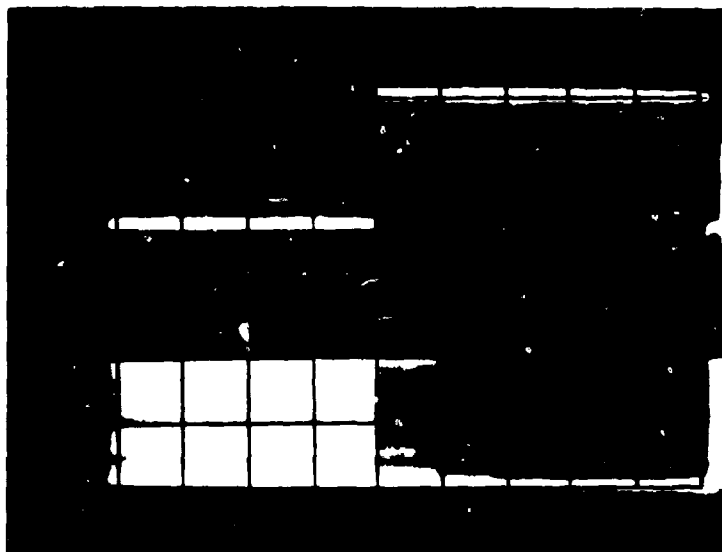
UPPER TRACE- POSITIVE
  TRANSITION GATES IF ON

LOWER TRACE- BIT ERROR
  OUTPUT, 5 ms/DIV

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Figure 53. 2 B/Hz Acquisition, IF Offset +20 kHz
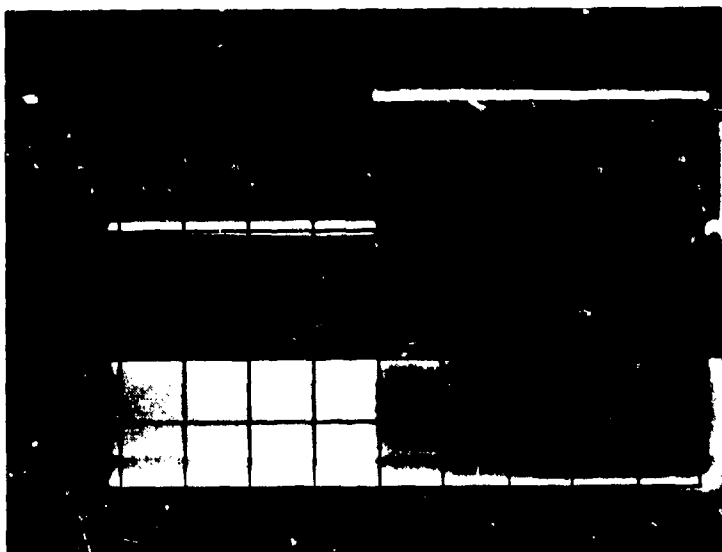
UPPER TRACE- POSITIVE
  TRANSITION GATES IF ON

LOWER TRACE- BIT ERROR
  OUTPUT, 5 ms/DIV

11/1/77

Figure 54. 2 B/Hz Acquisition, IF Offset -20 kHz
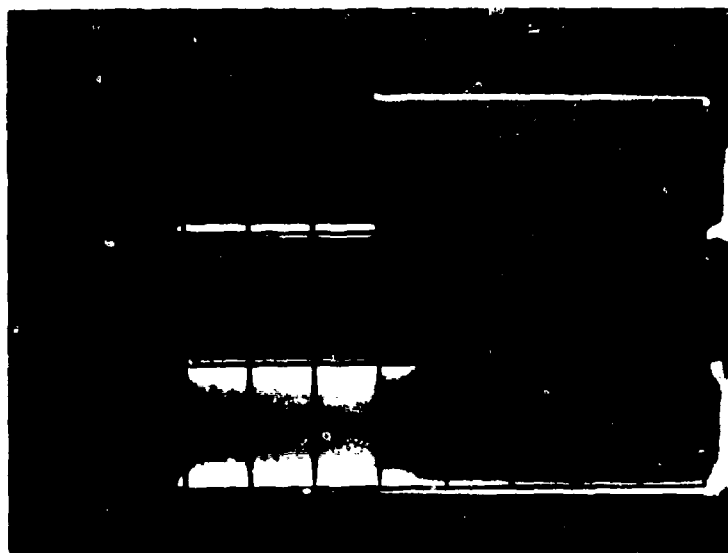
UPPER TRACE- POSITIVE
TRANSITION GATES IF ON

LOWER TRACE- BIT ERROR
OUTPUT, 5 ms/DIV

11/1/77

Figure 55. 1 B/Hz Acquisition, IF Offset +20 kHz
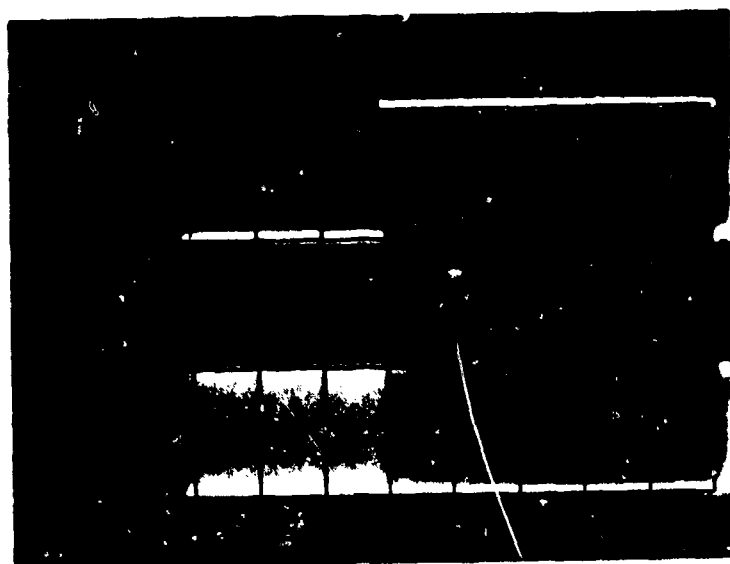
UPPER TRACE- POSITIVE
TRANSITION GATES IF ON

LOWER TRACE- BIT ERROR
OUTPUT, 5 ms/DIV

11/1/77

Figure 56. 1 B/Hz Acquisition, IF Offset -20 kHz

4.2   RADC Tests

This paragraph presents data acquired at the RADC test facility at Verona, New York, November 7, 1977 through November 11, 1977.

4.2.1   Spectral Efficiency Results

In order to demonstrate the spectral shaping introduced by the FCC 19311 waveguide filter, spectral measurements were first made at the output of the Philco Ford LC8D radio transmitter without the waveguide filter. The spectra were measured with a Hewlett Packard spectrum analyzer at 8 GHz. The analyzer was adjusted for 300 kHz IF bandwidth and 100 Hz video bandwidth and was used to drive an X-Y plotter. To ensure accuracy, the amplitude and frequency scales were calibrated with markers at 10 dB intervals on the vertical axis and with frequency markers at 0, ±7, and ±14 MHz on the horizontal axis. The 0 dB power reference was a single frequency tone from the modulator. This represents total transmitted power. All plots show a vertical axis that is corrected to a 4 kHz IF bandwidth. The correction factor for a bandwidth reduction from 300 kHz to 4 kHz is -18.8 dB, hence the nonintegral calibration marks.

Figure 57 shows the unfiltered 2 B/Hz spectrum at the transmitter output. The FCC 19311 spectral mask is drawn to scale on the plot. The two side lobes exceed allowable levels by some 12 dB indicating that additional filtering is required. Figure 58 shows the unfiltered 1 B/Hz spectrum. Its side lobes also exceed allowable levels by approximately 10 dB.

The spectra were remeasured after installation of the FCC 19311 waveguide filter at the radio transmitter output. Figure 59 and Figure 60 show the 2 B/Hz spectrum and 1 B/Hz spectrum respectively. The 2 B/Hz spectrum fits within the spectral mask with a minimum margin of approximately 4.4 dB. The 1 B/Hz spectrum has a margin of approximately 7.5 dB. Thus, the spectral requirements of FCC Docket 19311 are met.

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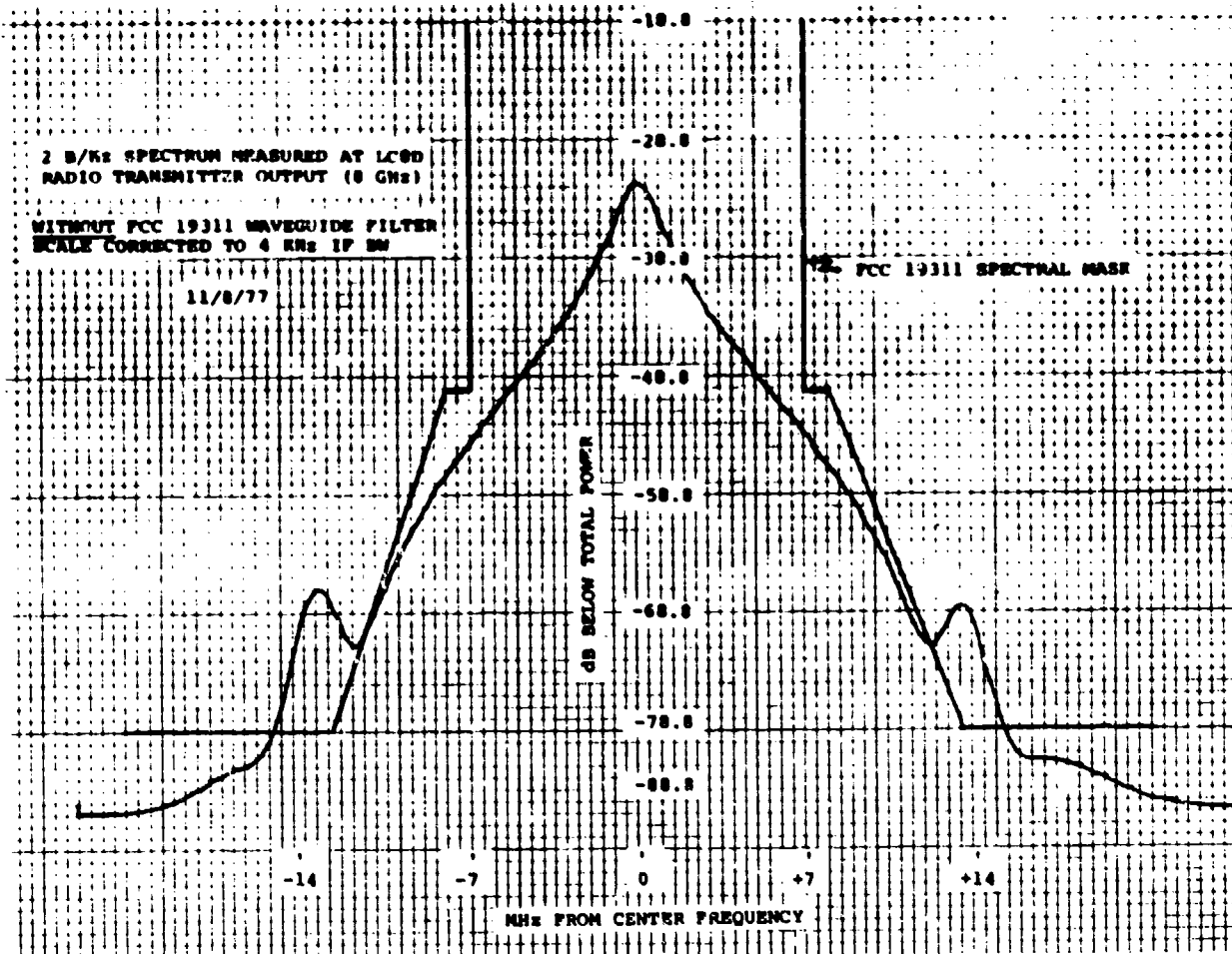
Figure 57. 2 B/Hz Spectrum Measured at LC8D Radio Transmitter
Output (8 GHz) Without FCC 19311 Waveguide Filter

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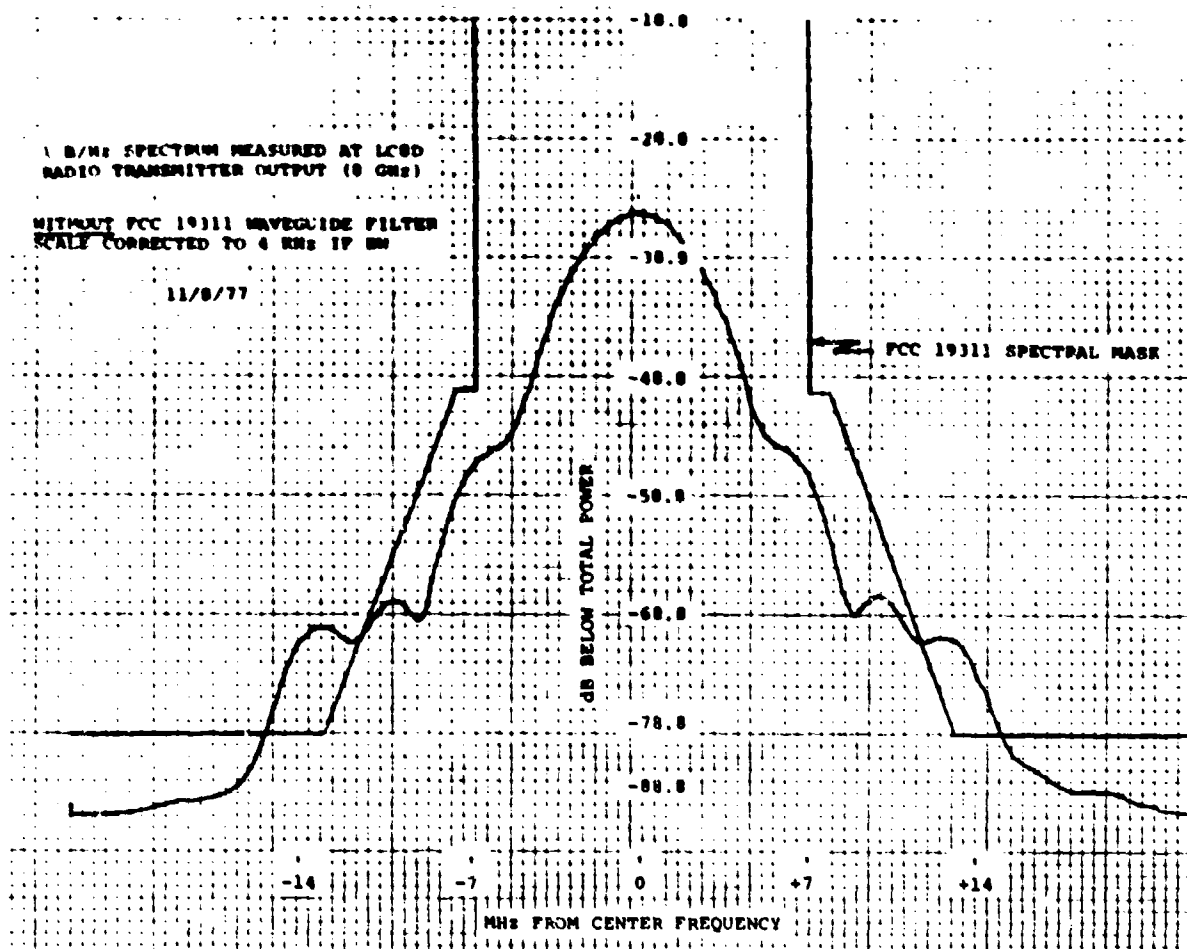
Figure 58. 1 B/Hz Spectrum Measured at LC8D Radio Transmitter Output (8 GHz) Without FCC 19311 Waveguide Filter

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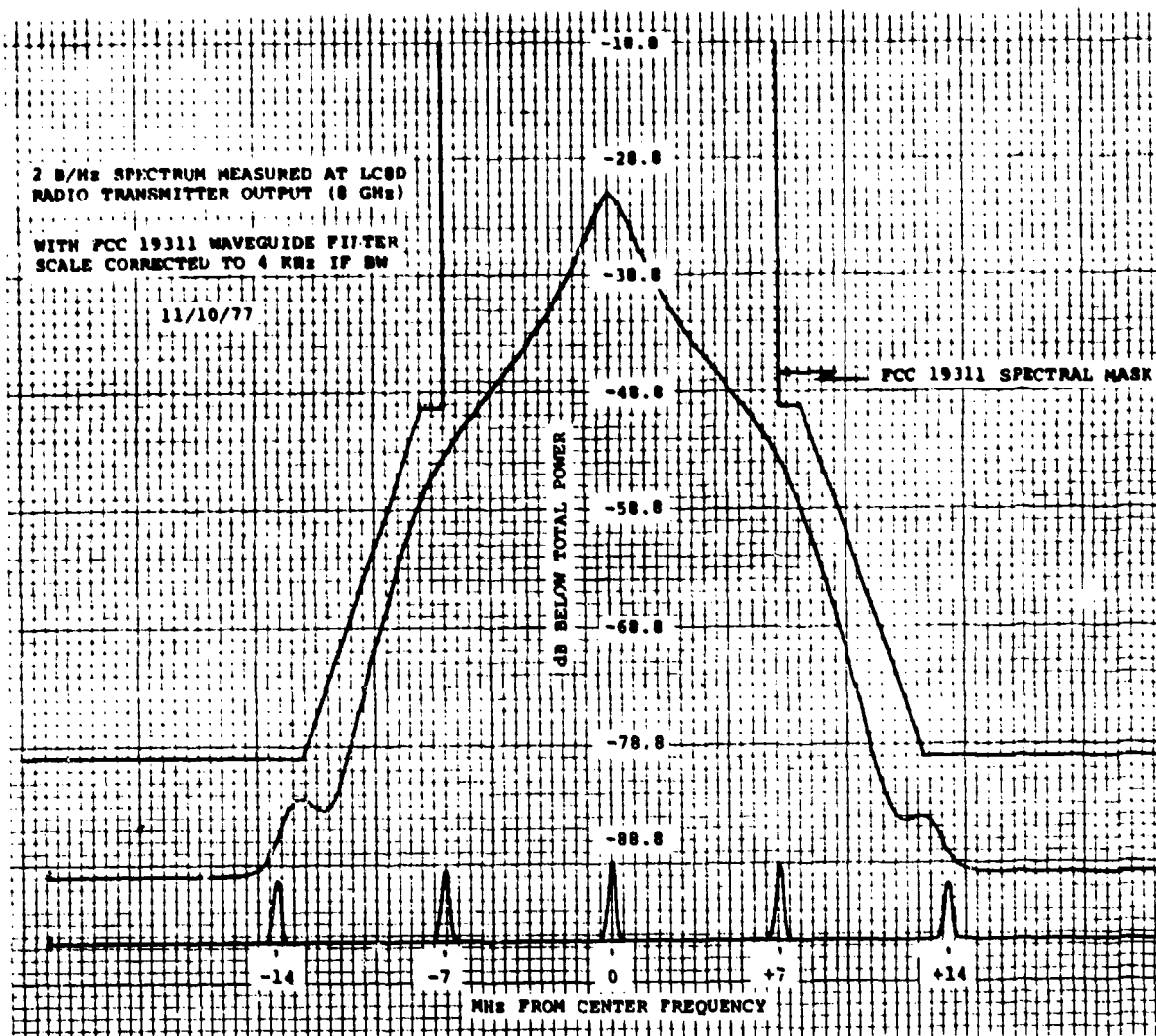
Figure 59. 2 B/Hz Spectrum Measured at LC8D Radio Transmitter
Output (8 GHz) With FCC 19311 Waveguide Filter
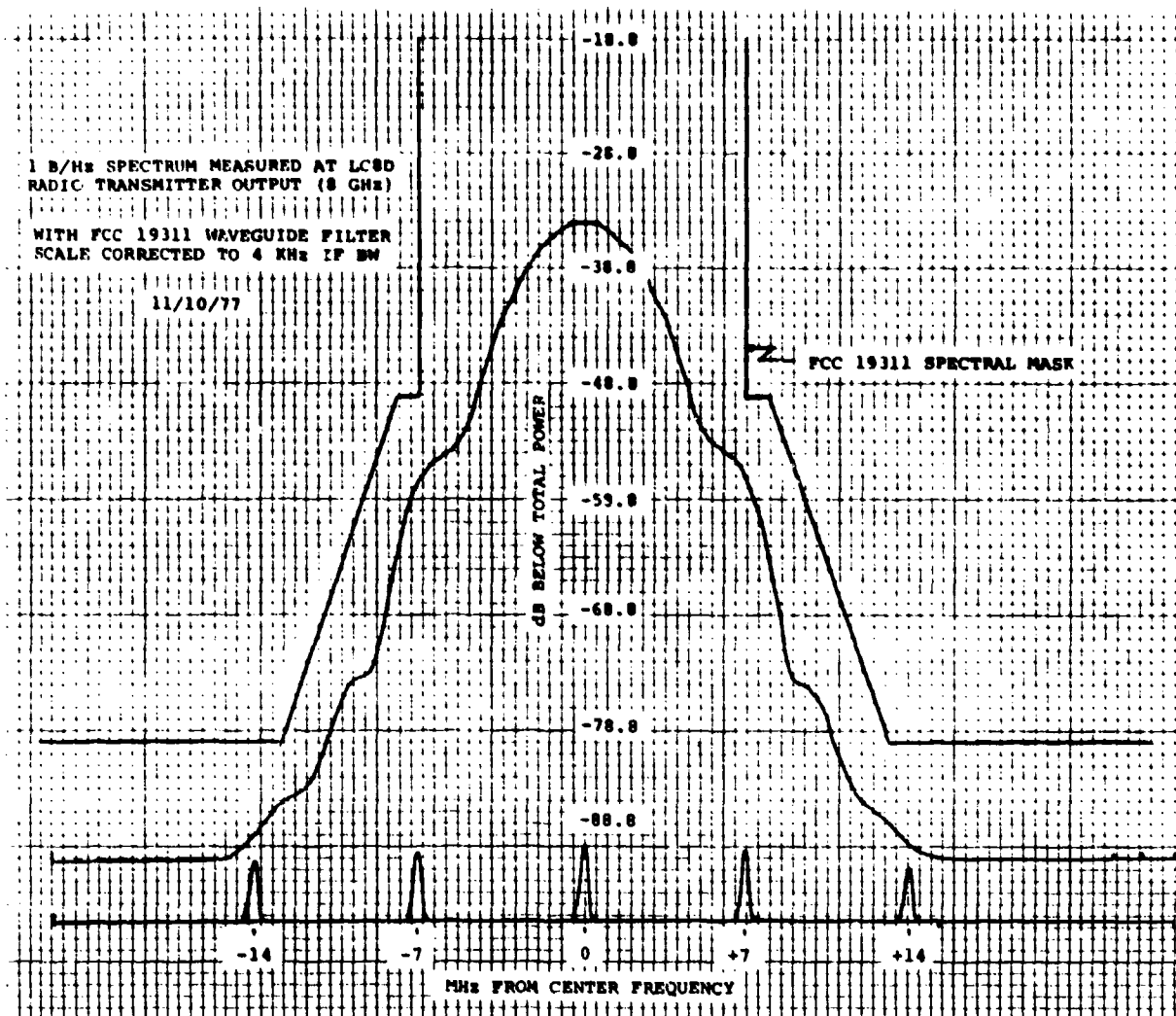
Figure 60. 1 B/Hz Spectrum Measured at LC8D Radio Transmitter
Output (8 GHz) With FCC 19311 Waveguide Filter

It was noted that the measured peak of the spectra (at center frequency) is 3 to 4 dB lower than predicted by computer simulation. This was also observed on the photographs taken at Harris ESD. The discrepancy may perhaps be attributed to the operation of the spectrum analyzer which averages the log of the signal rather than averaging the signal before taking the log. However, even if the spectral plots are shifted upwards by 4 dB, they still fit within the FCC 19311 mask.

The spectra were also measured at the radio receiver IF output. Though the curves still fall below the FCC 19311 mask, the side lobes are somewhat stronger than those measured at 8 GHz. This is probably the result of limiting due to overload at the receiver downconverter. Tests were run with maximum signal level through the simulator. The spectral plots at the receiver IF are shown in Figures 61 and 62.

4.2.2 BER Versus E_b/N_o Results

Bit error rate tests were run with the modem as received from shipment. No attempt was made to realign the modem to optimize its performance. The design objective was a BER of 5×10^{-9} or less at an E_b/N_o of 22 dB over the LC8D radio in the 2 B/Hz mode. For the 1 B/Hz mode, the objective was 5×10^{-9} at an E_b/N_o of 16 dB. These objectives were for operation without the randomizer which degrades performance by a factor close to three. The BER performance was measured in a variety of configurations, as described below. Unless otherwise noted, measurements were made with noise added at IF as with the in-plant tests at Harris ESD. This gave more repeatable results than the radio noise technique described in the Test Plan. Tests with radio noise were run, however, as a check on the validity of the IF noise measurement technique, and the results are included in this section.

4.2.2.1 2 B/Hz Test Results

Baseline performance data was obtained with a 70 MHz back-to-back test with additive Gaussian noise. The result is shown in Figure 63. The test was run with the randomizer operating. A BER of 5×10^{-9} was achieved at an E_b/N_o of 21.1 dB. This represents a
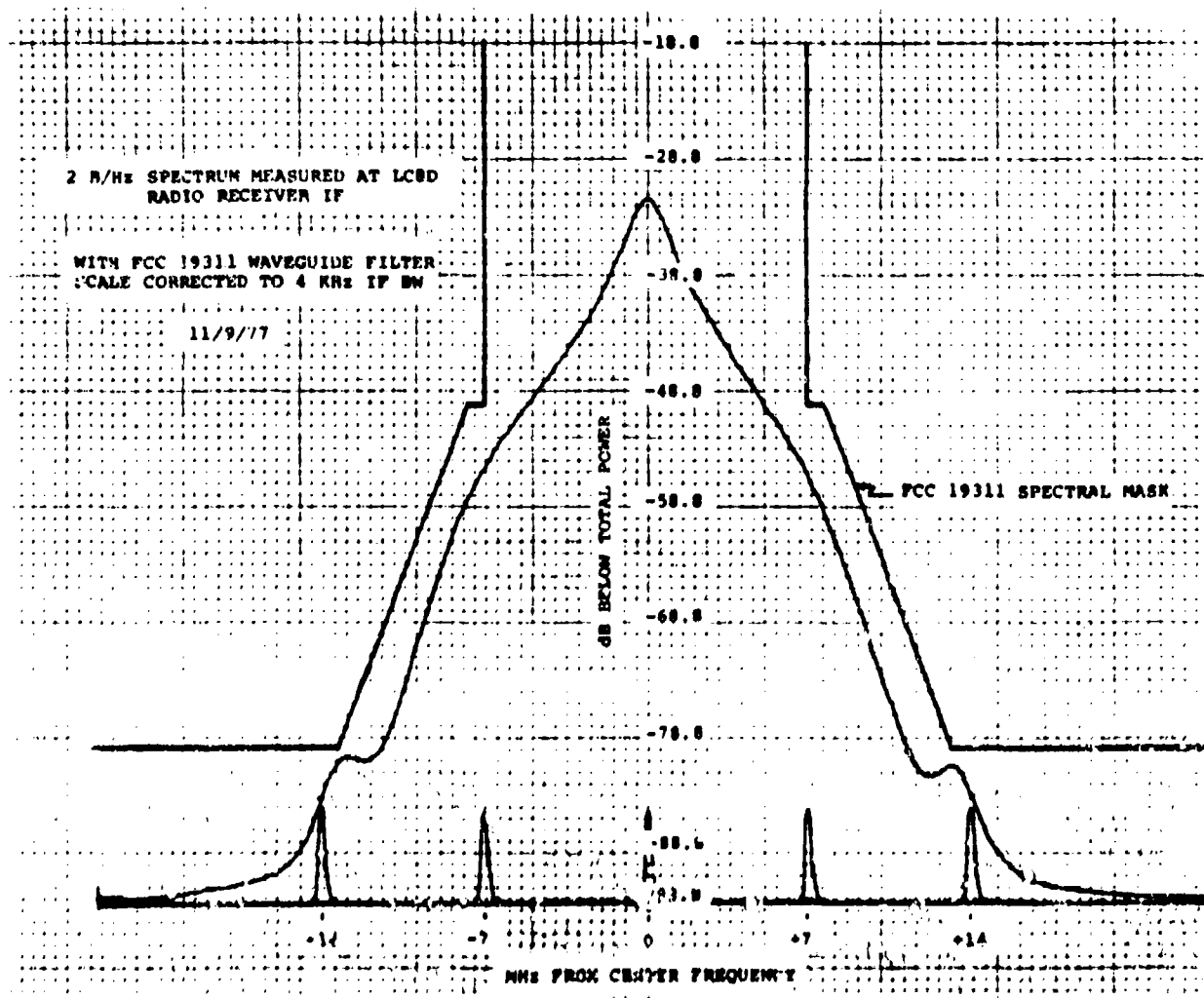
Figure 61. 2 B/Hz Spectrum Measured at LC8D Radio Receiver IF With FCC 19311 Filter
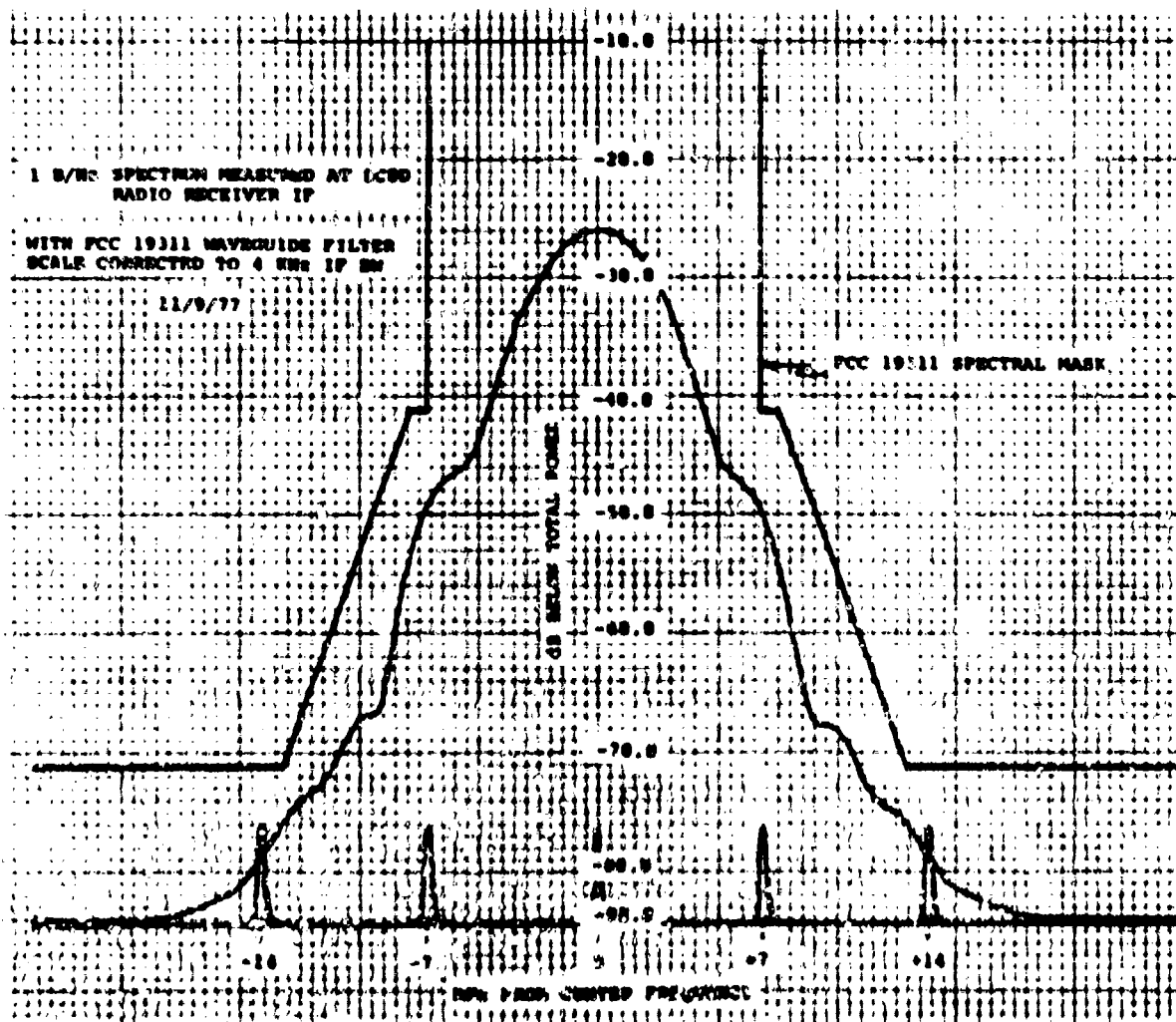
Figure 62. 1 B/Hz Spectrum Measured at LC8D
Radio Receiver IF With FCC 19311 Filter
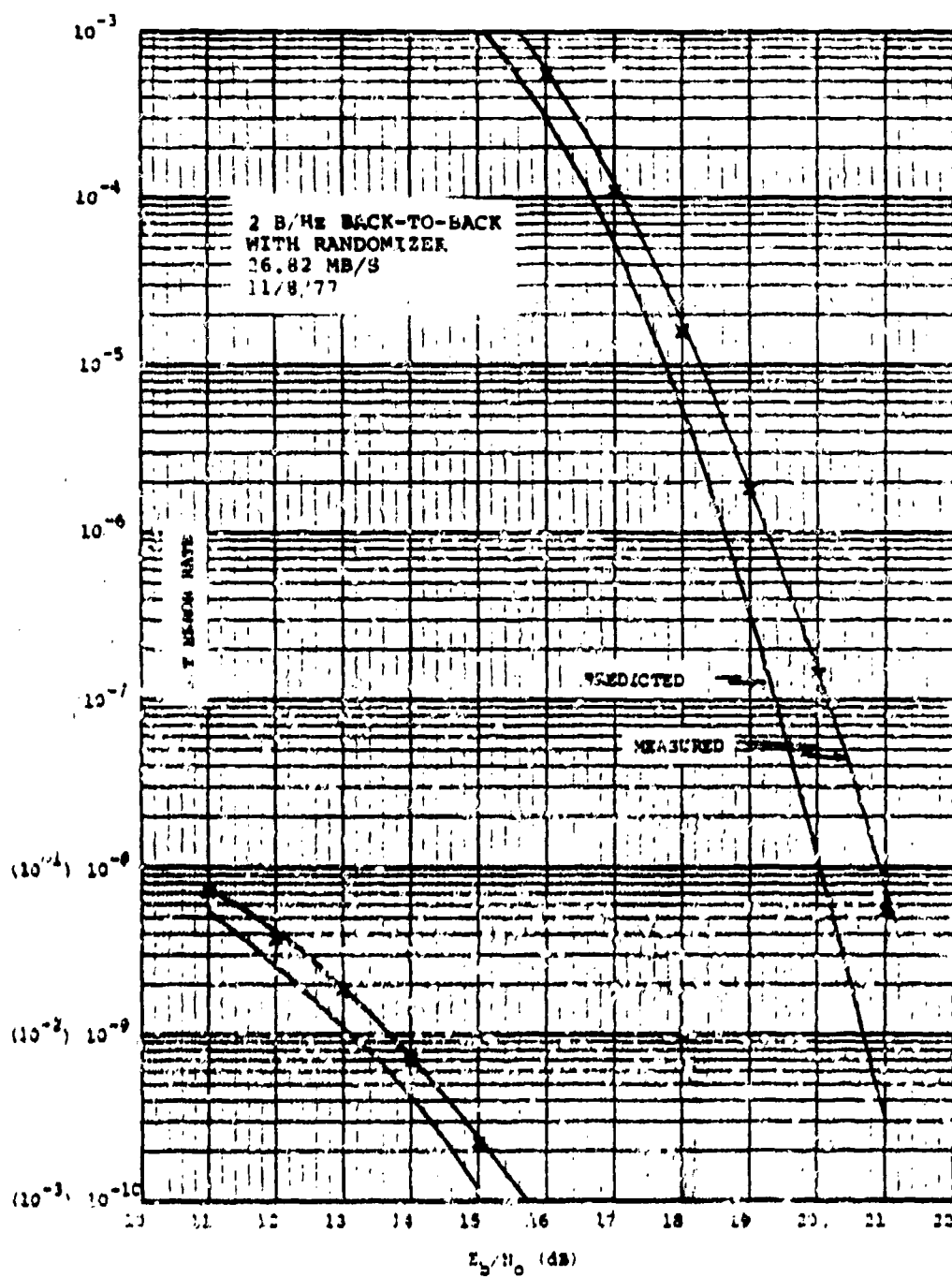
Figure 63. BER-2 B/Hz, Back-to-Back, With Randomizer

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degradation of approximately 0.2 dB from that measured during the in-plant tests at Harris ESD. This is close to measurement accuracy and represents excellent stability through shipping.

The second test at RADC was operation through the LCBD radio and simulator without the FCC 19311 waveguide filter. The simulator connected the radio back-to-back. Thermal noise was added to the radio IF output for E_b/N_0 calibration. The simulator was set for minimum signal attenuation and the modem randomizer was utilized. An external data source and error detector were used for convenience in measurement. A BER of 5×10^{-9} was measured at an E_b/N_0 of 21.5 dB. The complete curve is shown in Figure 64.

The above test was then repeated with the FCC 19311 waveguide filter installed in the LCBD radio transmitter. The resulting curve is shown in Figure 65. A BER of 5×10^{-9} occurred at an E_b/N_0 of 23.2 dB. The randomizer was then bypassed so that the results could be compared more easily with those obtained at Harris ESD with the up/downconverter. This curve is shown in Figure 66. A BER of 5×10^{-9} was measured at an E_b/N_0 of 23.2 dB as before. The factor of three improvement did not materialize due to error in measurement repeatability. This is within 0.3 dB of that obtained at Harris ESD with the up/downconverter (Figure 48).

Figure 67 shows the BER performance with randomizer through the radio with FCC 19311 filter and AGC amplifier. Comparison with Figure 65 reveals that the IF AGC amplifier in the LCBD degrades performance by approximately 0.6 dB in the vicinity of a 10^{-8} BER. The AGC amplifier was found to introduce additional group delay distortion that is a function of amplifier gain (and, hence, receive level). Distortion peaks at maximum received level (minimum gain). A plot of performance with the AGC amplifier but without randomizer is shown in Figure 68. A BER of 5×10^{-9} was achieved at an E_b/N_0 of 23.4 dB without group delay compensation. This is 1.4 dB from the design objective.

Figure 64. BER-2 B/Hz, LCBD Radio, Without FCC 19311
Waveguide Filter, With Randomizer

Figure 65.   BER-2 B/Hz, LCBD Radio, With FCC 19311
Waveguide Filter and Randomizer

Figure 66. BER-2 B/Hz, LC8D Radio, With FCC 19311 Waveguide
Filter, Without Randomizer

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Figure 67. BER-2 B/Hz, LCBD Radio, With FCC 18311 Waveguide Filter, AGC Amplifier and Randomizer

Figure 68.   BER-2 B/Hz, LC8D Radio, With FCC 19311 Waveguide
           Filter and AGC Amplifier, Without Randomizer

An attempt was made to equalize the LC80 radio at IF with the FCC 19311 waveguide filter and AGC amplifier installed. A plot of amplitude response and group delay before equalization is shown in Figure 69. A single section of group delay equalization $(4/25$ ns/MHz^2 parabolic) provided considerable improvement as can be seen in Figure 70. BER performance with this equalization is shown in Figure 71. A BER of 5×10^{-9} was measured at an E_b/N_0 of 22.6 dB. This is only 0.6 dB from the design goal and represents an improvement of 1.0 dB over the unequalized radio (Figure 67). Note that the data in Figure 71 was obtained with randomizer. The design objective with randomizer becomes 1.5×10^{-8} BER at an E_b/N_0 of 22 dB. This bit error rate was achieved at an E_b/N_0 of 22.2 dB. Thus, performance with the equalized radio is essentially within 0.2 dB of the design objective.

Further attempts to improve the equalization did not improve BER performance significantly. Optimum group delay and amplitude response were achieved with the following equalization sections:

(1) $4/25$ ns/(MHz)^2 parabolic group delay

(2) $-6/10$ ns/MHz linear group delay

(3) $+0.2$ dB/MHz amplitude

(4) $+0.1$ dB/MHz amplitude

As a check on the test set which added Gaussian noise at IF, two curves were run using the noise coming from the radio itself and attenuating the received power level in the simulator to adjust E_b/N_0. Calibration was achieved by measuring radio noise alone and then increasing signal power until that level increased by 3 dB, thus setting the 0 dB S/N point. Corrections were then made to determine E_b/N_0 based on the noise filter bandwidth. Calibration by this method was found to be less repeatable than with the IF test set and was probably accurate only to within ± 0.5 dB. Figure 72 shows results with radio noise and unequalized radio. Figure 73 shows results with radio noise on the equalized radio. Both curves shows a BER of 5×10^{-9} at an E_b/N_0 near 22.4 dB. No gain is shown using equalization but this is a result of calibration error
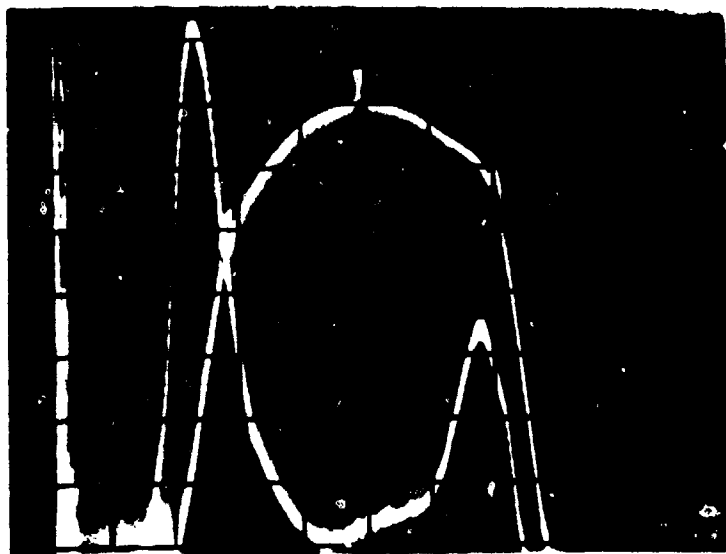
UPPER TRACE- AMPLITUDE
    RESPONSE, 2 dB/DIV,
    MARKERS AT ± 7 MHz

LOWER TRACE- GROUP DELAY,
    5 ns/DIV

11/9/77

Figure 69.   Amplitude Response and Group Delay of LC8D With
         FCC 19311 Filter, Without Equalization
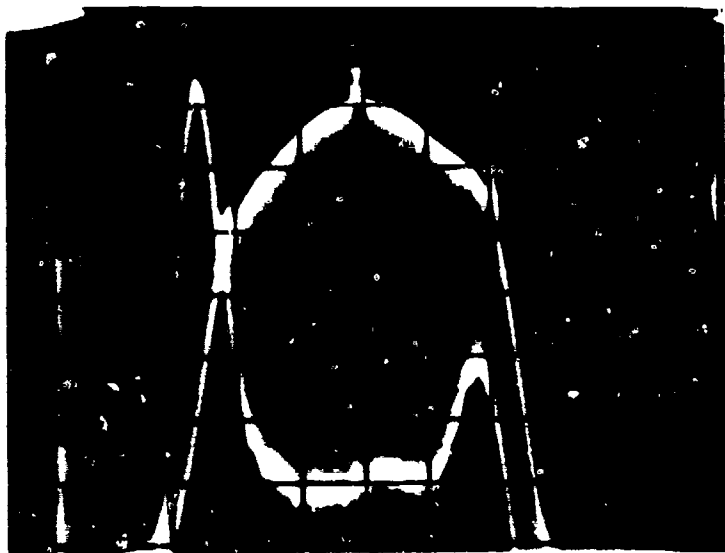
LC8D WITH FCC 19311_2FILTER
    WITH 4/25 ns/MHz^2
    PARABOLIC EQUALIZATION

UPPER TRACE- AMPLITUDE
    RESPONSE, 2 dB/DIV
    MARKERS AT ± 7 MHz

LOWER TRACE- GROUP DELAY,
    5 ns/DIV

11/9/77

Figure 70.   Amplitude Response and Group Delay of LC8D With FCC 19311
      Filter, with 4/25 ns/MHz^2 Parabolic Group Delay Equalization

Figure 71. BER-2 B/Hz, LCSD Radio, With FCC 19311 Waveguide Filter, AGC
Amplifier, Randomizer, and 4/25 ns/MHz^2 Parabolic Equalization

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Figure 72.   BER-2 B/Hz, LC8D Radio, With FCC 19311 Waveguide
Filter, AGC Amplifier, Randomizer, and Radio Noise

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Figure 73.   BER 2 B/Hz, LC8D Radio, With FCC 19311 Waveguide Filter, AGC
Amplifie   Randomizer, 4/25 ns/MHz^2 Parabolic Equalization,
and Radio Noise

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using this technique. However, results do compare within measurement
accuracy to those obtained with IF noise, demonstrating the validity of the
measurement technique.

4.2.2.2   1 B/Hz Results

The 1 B/Hz back-to-back performance as measured with additive IF
noise is depicted in Figure 74. A 5×10^{-9} BER was measured with
randomizer at an E_b/N_0 of 15.9 dB. Through the radio without FCC 19311
filtering, this BER occurred at an E_b/N_0 of 16 dB as seen in Figure
75. The addition of the FCC 19311 waveguide filter degraded performance by
approximately 0.4 dB as shown in Figure 76. The curve measured through the
radio and filter but without randomizer is shown in Figure 77. A BER of
5×10^{-9} was achieved at an E_b/N_0 of 15.9 dB. This is slightly
better than the design objective.

The addition of the 70 MHz IF AGC amplifier in the Philco Ford
LC8D had little effect on performance. The shift in the curves could be
attributed to variations in measurement. Figure 78 shows the measured data
with randomizer and Figure 79 without. Performance with randomizer
actually measures slightly better (approximately 0.1 dB) with AGC than
without. The data for the two cases were taken on different days, however,
and this can easily acccount for the apparent discrepancy. Performance
without the randomizer measures approximately 0.25 dB worse with AGC than
without (Figures 79 and 77 respectively). As these two sets of data were
taken the same day, they are probably inicative of the actual degradation
caused by the AGC. Without randomizer but with 19311 filtering and AGC, a
BER of 5×10^{-9} was measured at an E_b/N_0 of 16.2 dB.

The $4/25$ ns/MHz^2 parabolic group delay equalization that
gained approximately 1.0 dB in 2 B/Hz BER performance had little effect on
1 B/Hz BER performance. A plot of data taken through the equalized radio
with AGC and randomizer is shown in Figure 80. A BER of 5×10^{-9}
occurred at an E_b/N_0 of 16.3 dB. If one assumes a degradation of a
factor of three for the randomizer, the design objective becomes
1.5×10^{-8} at 16 dB. Figure 80 shows that this is narrowly met.
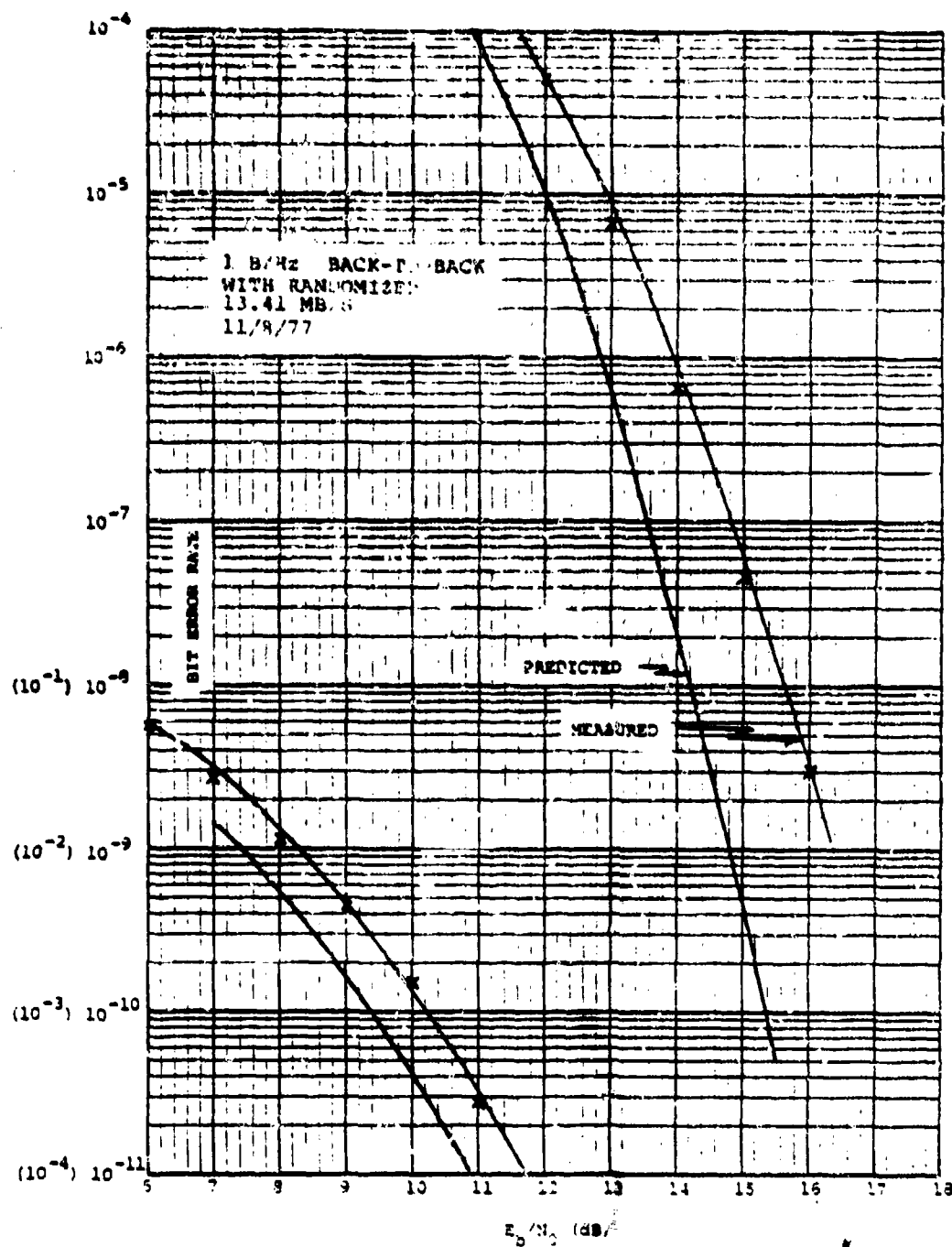
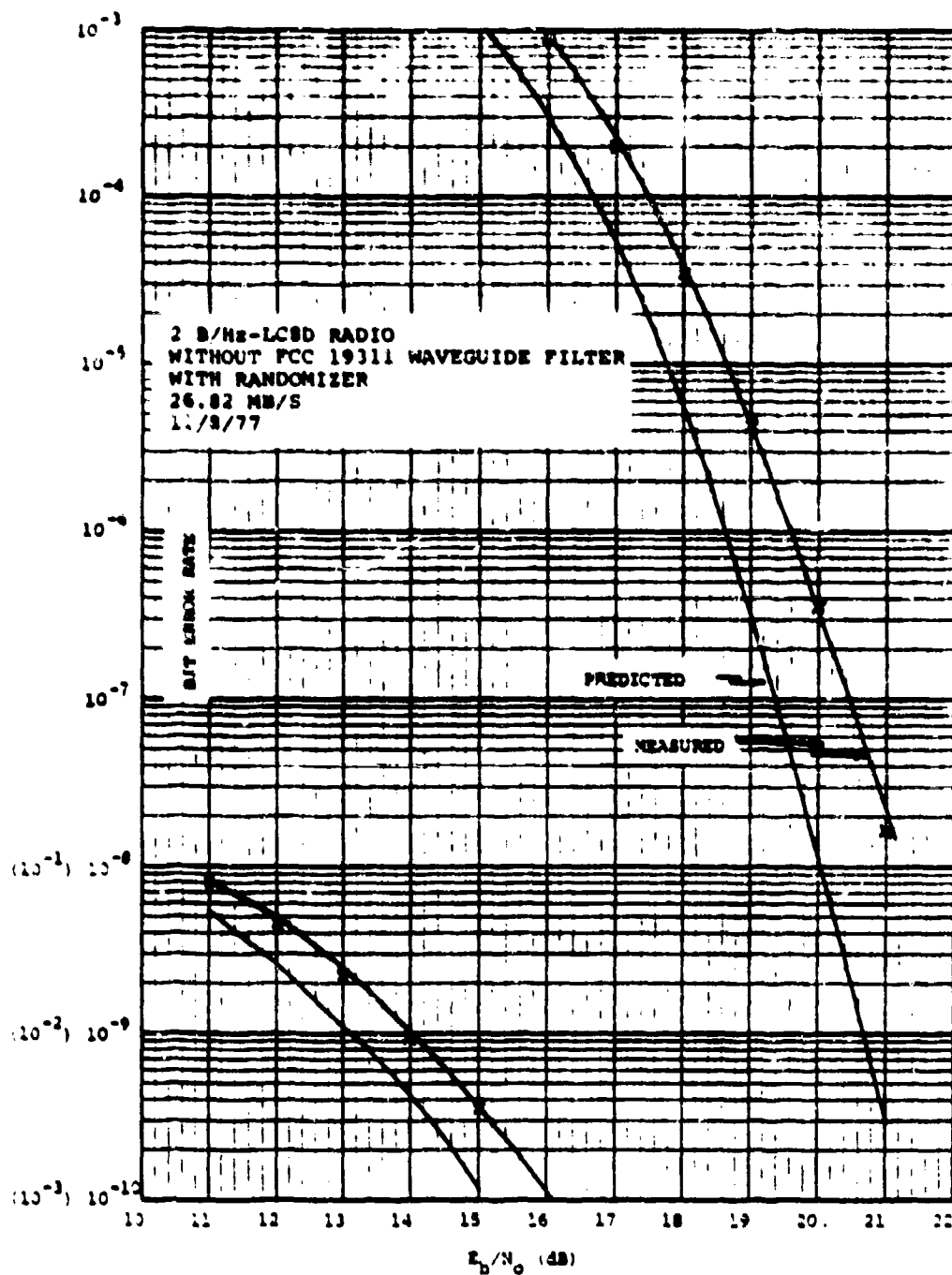Figure 74. BER-1 B/Hz, Back-to-Back, With Randomizer

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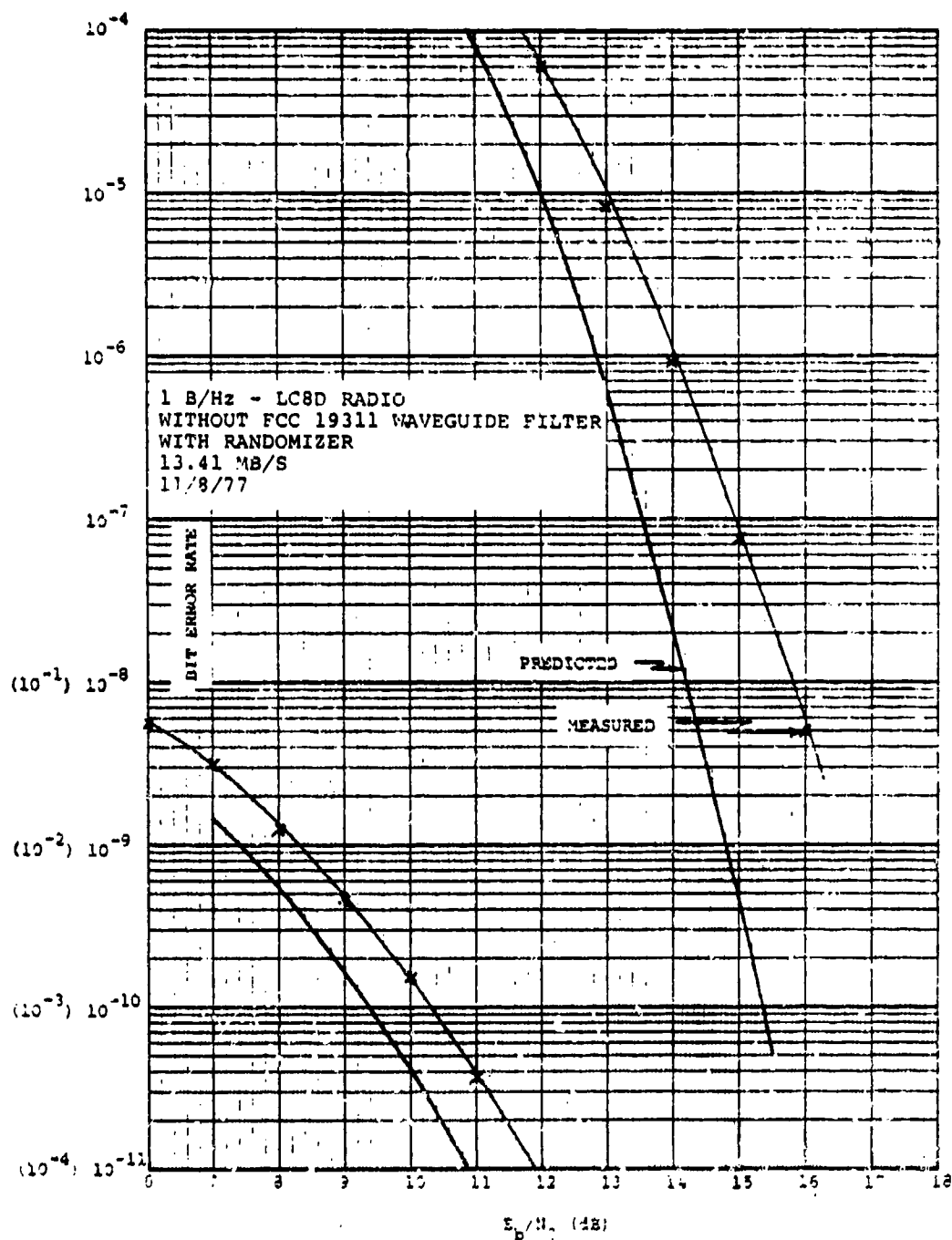
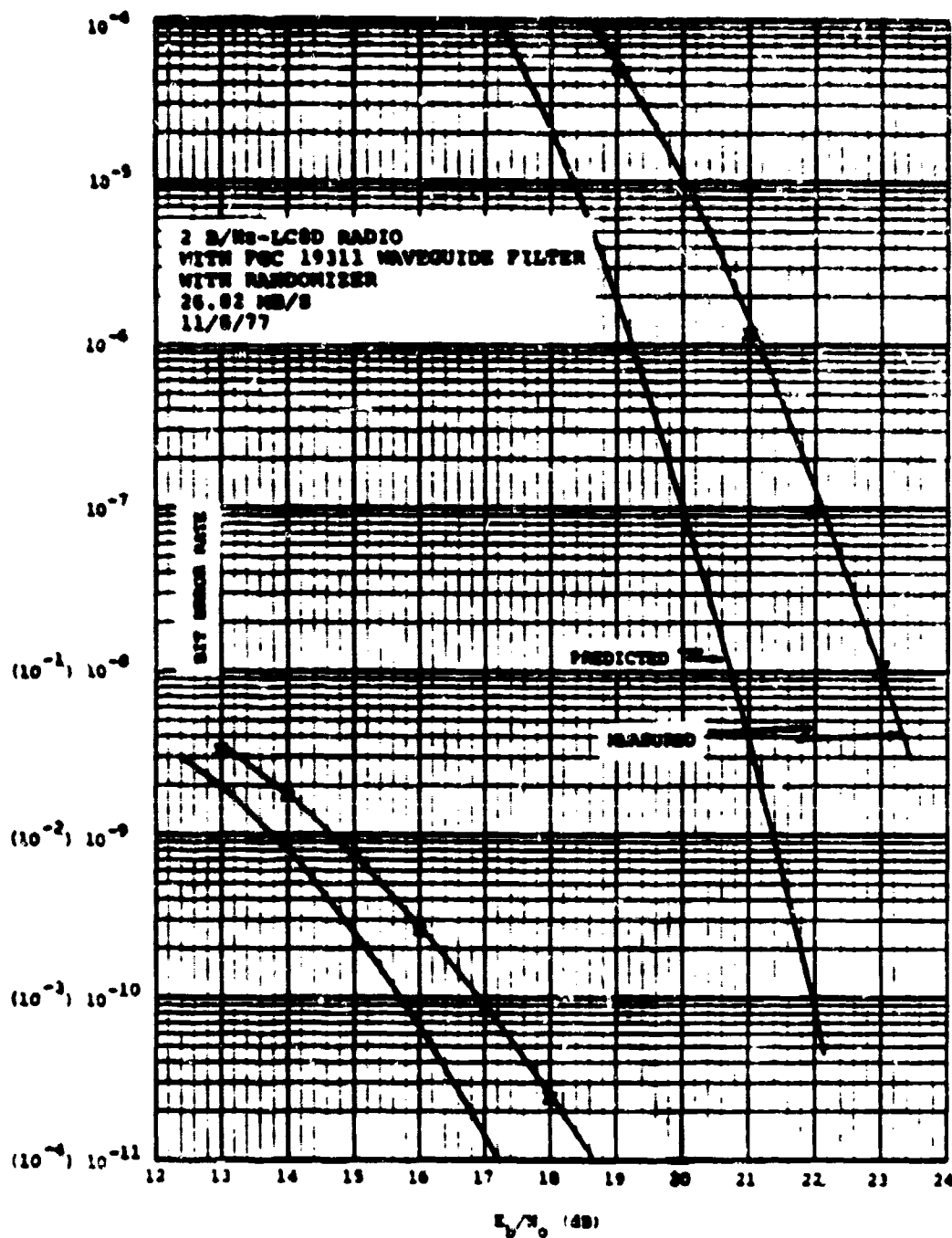Figure 75. BER-1 B/Hz, LC8D Radio, Without FCC 19311 Waveguide Filter, With Randomizer
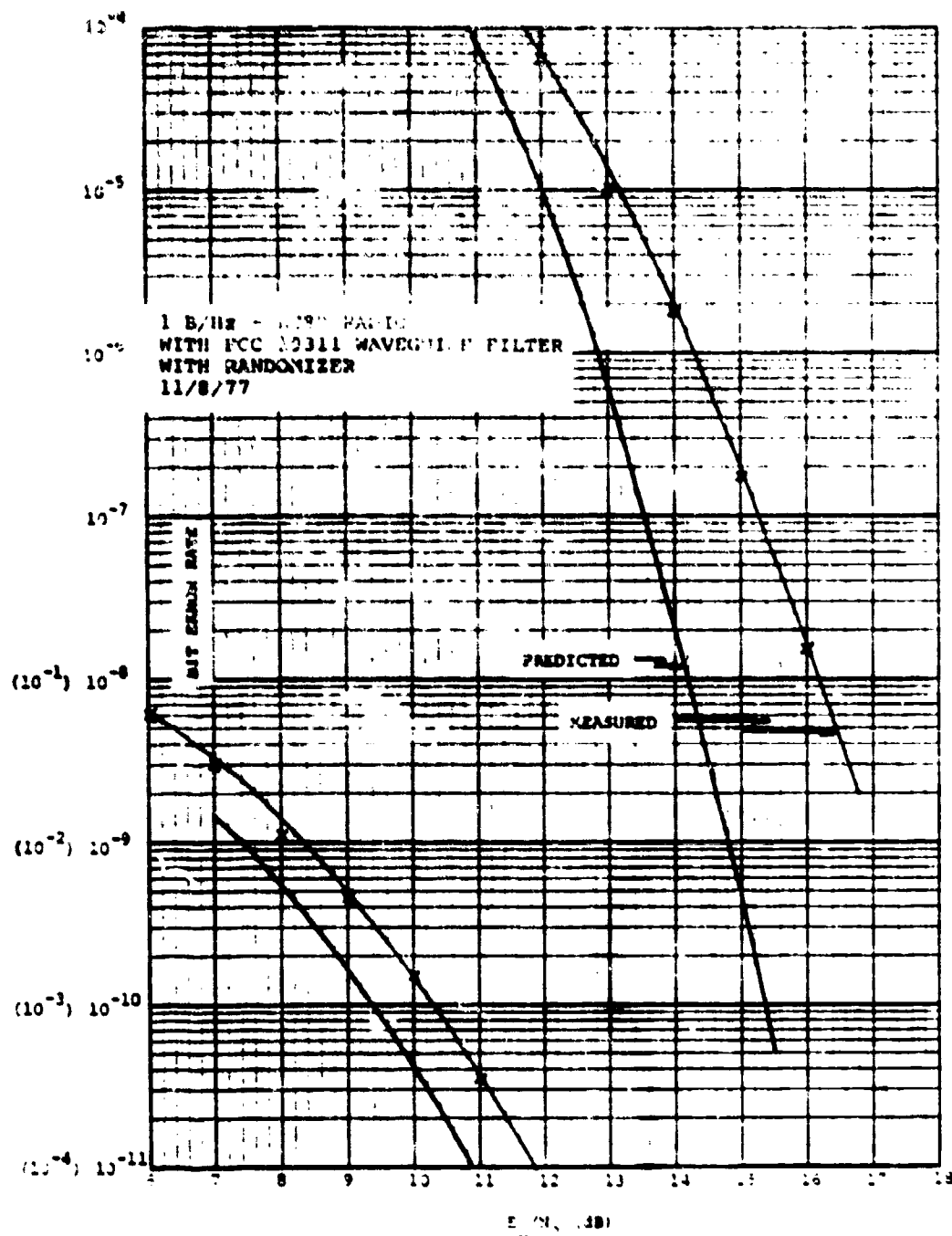
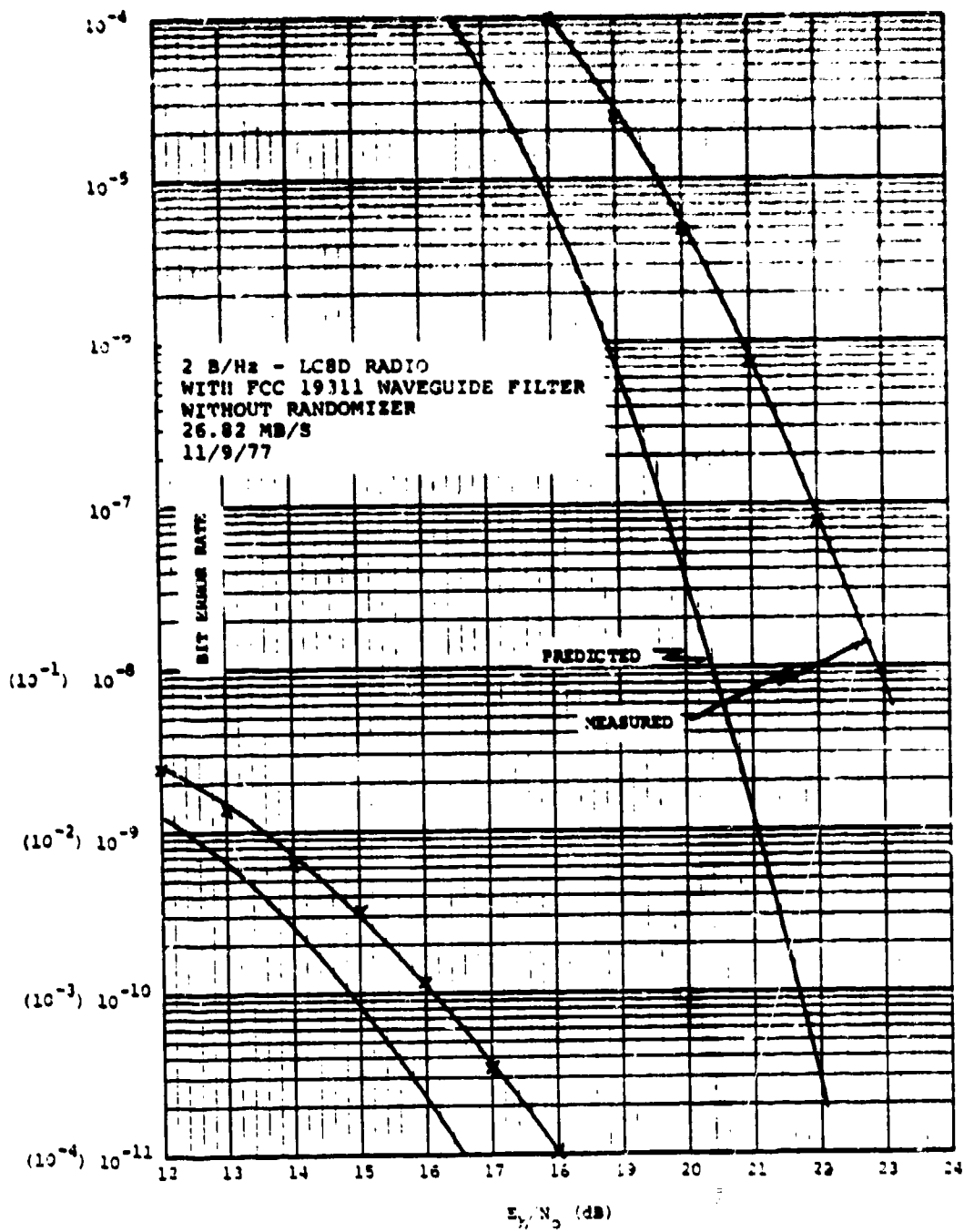Figure 76. BER-1 B/H:, LC8D Radio, With FCC 19311 Waveguide Filter and Randomizer
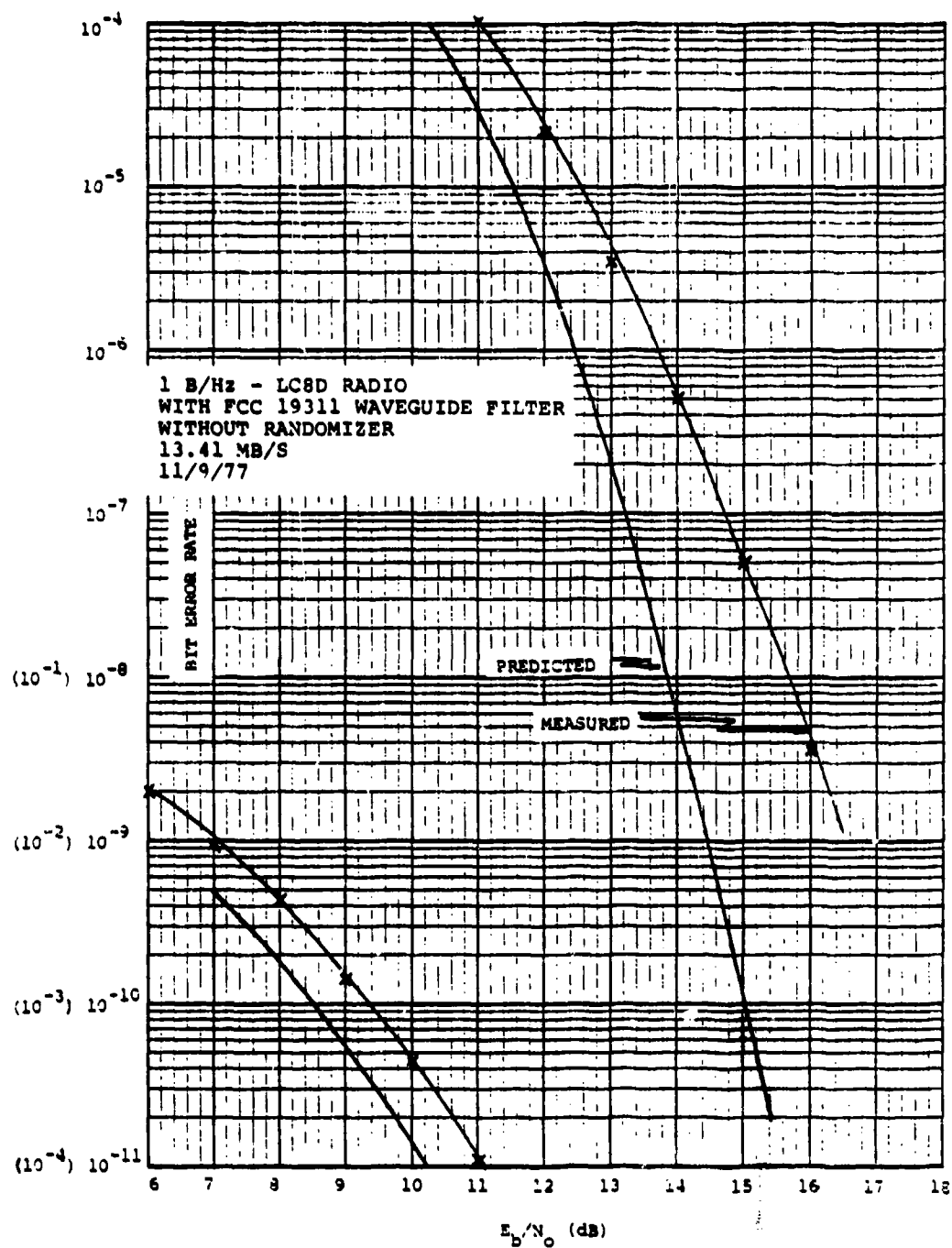
Figure 77.   BER-1 B/Hz, LC8D Radio, With FCC 19311 Waveguide
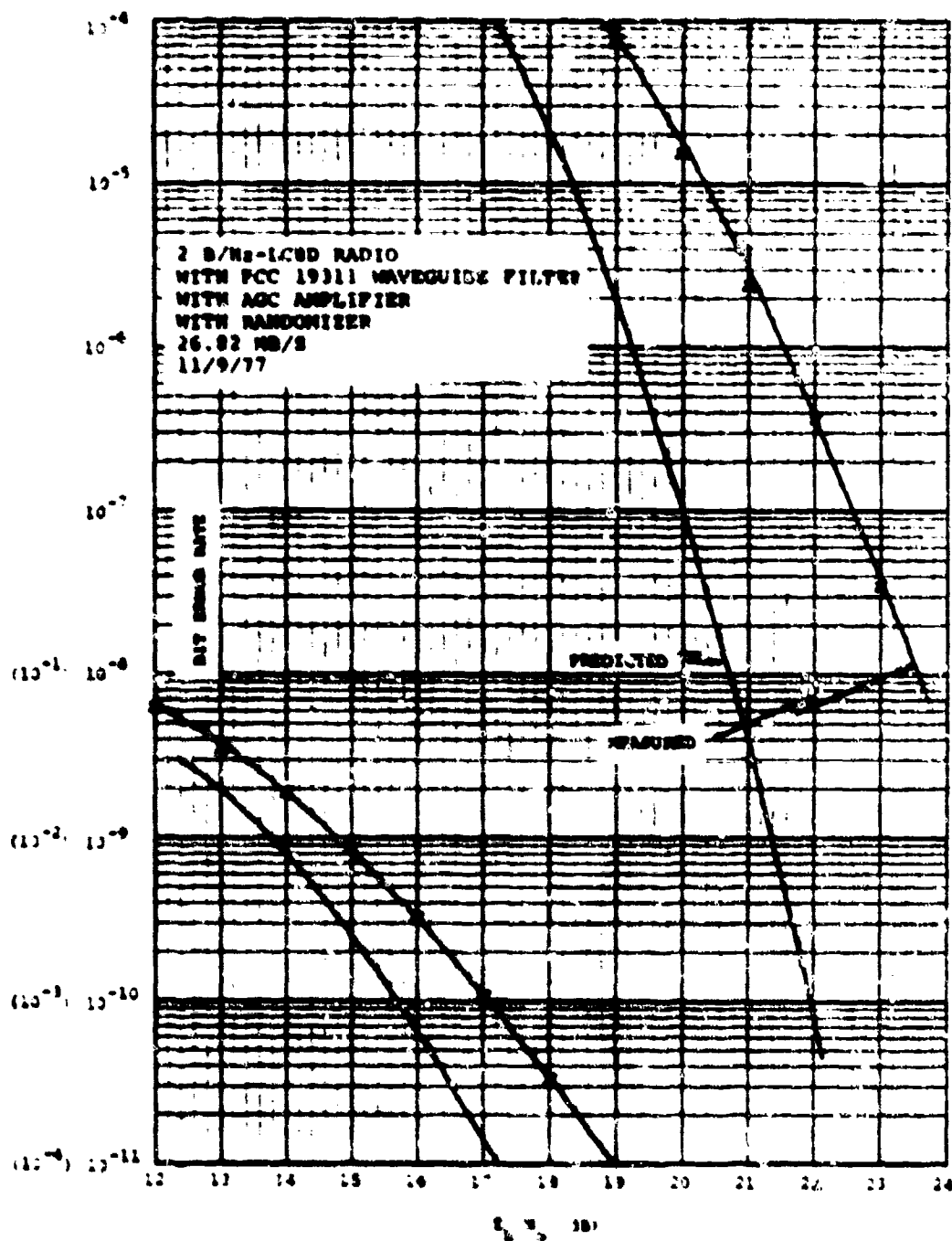Filter, Without Randomizer
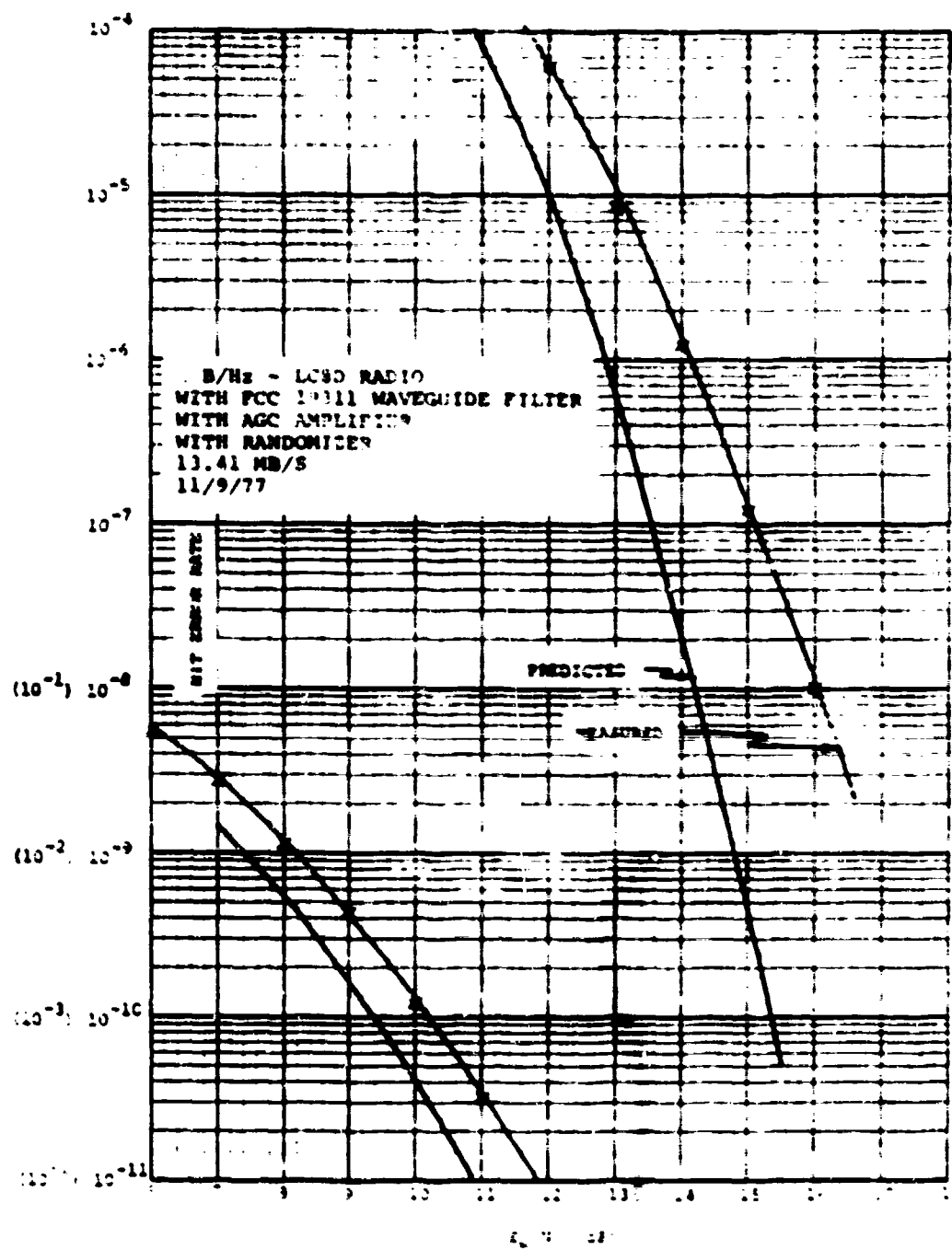
Figure 78. BER-1 B/Hz, LC8D Radio, With FCC 19 11 Waveguide
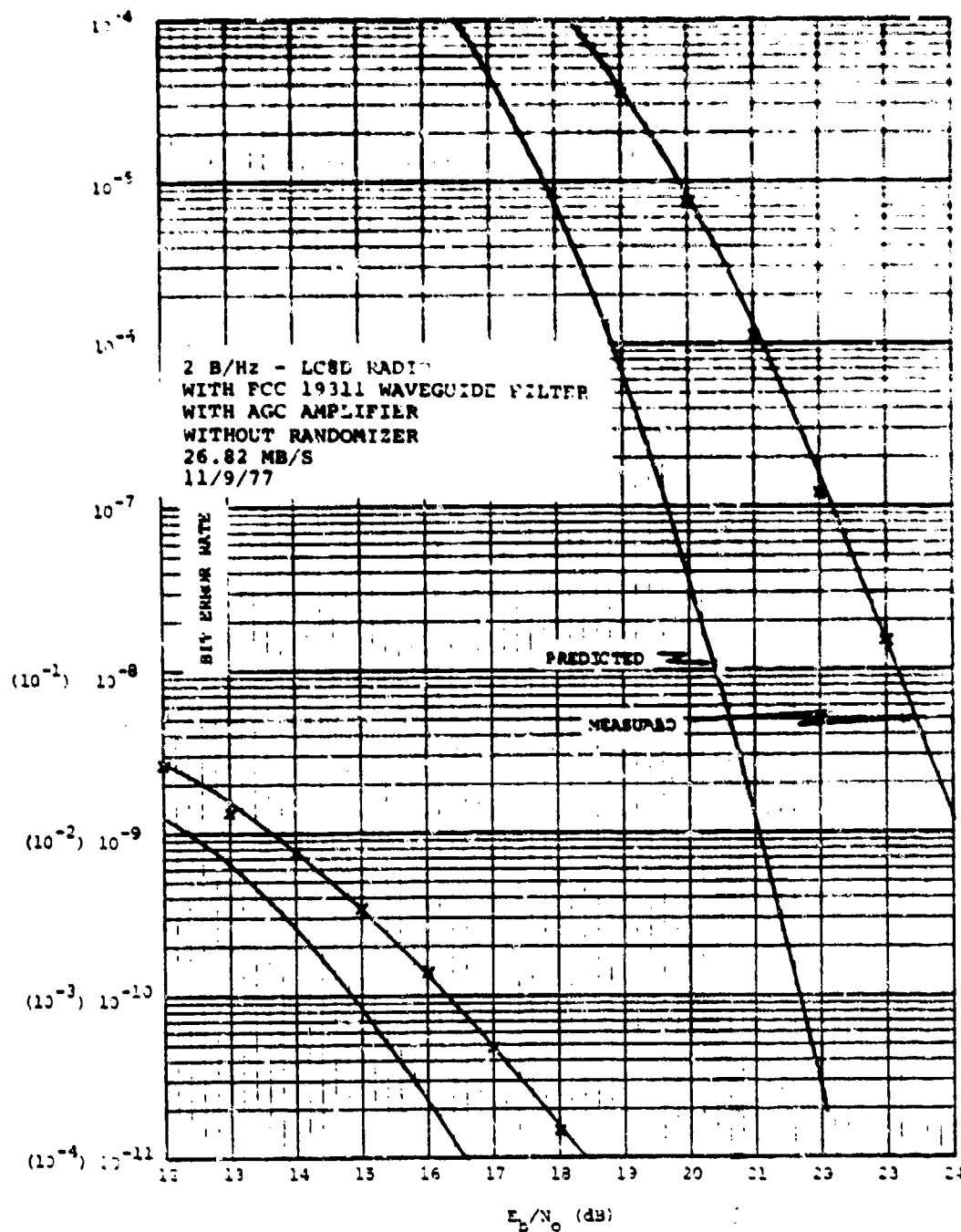Filter, AGC Amplifier, and Randomizer
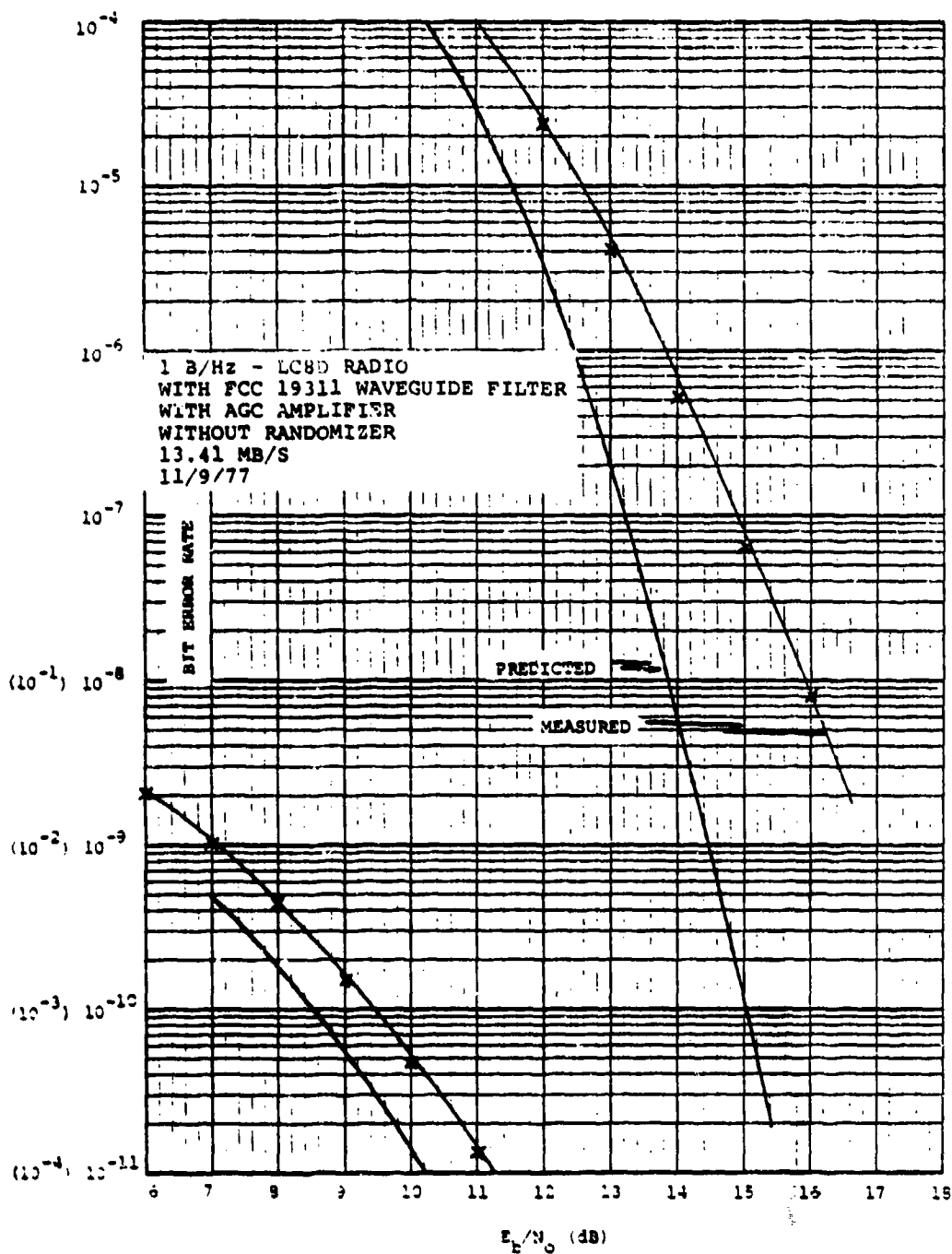
Figure 79. BER-1 B/Hz, LC8D Radio, With FCC 19311 Waveguide
Filter, and AGC Amplifier, Without Randomizer

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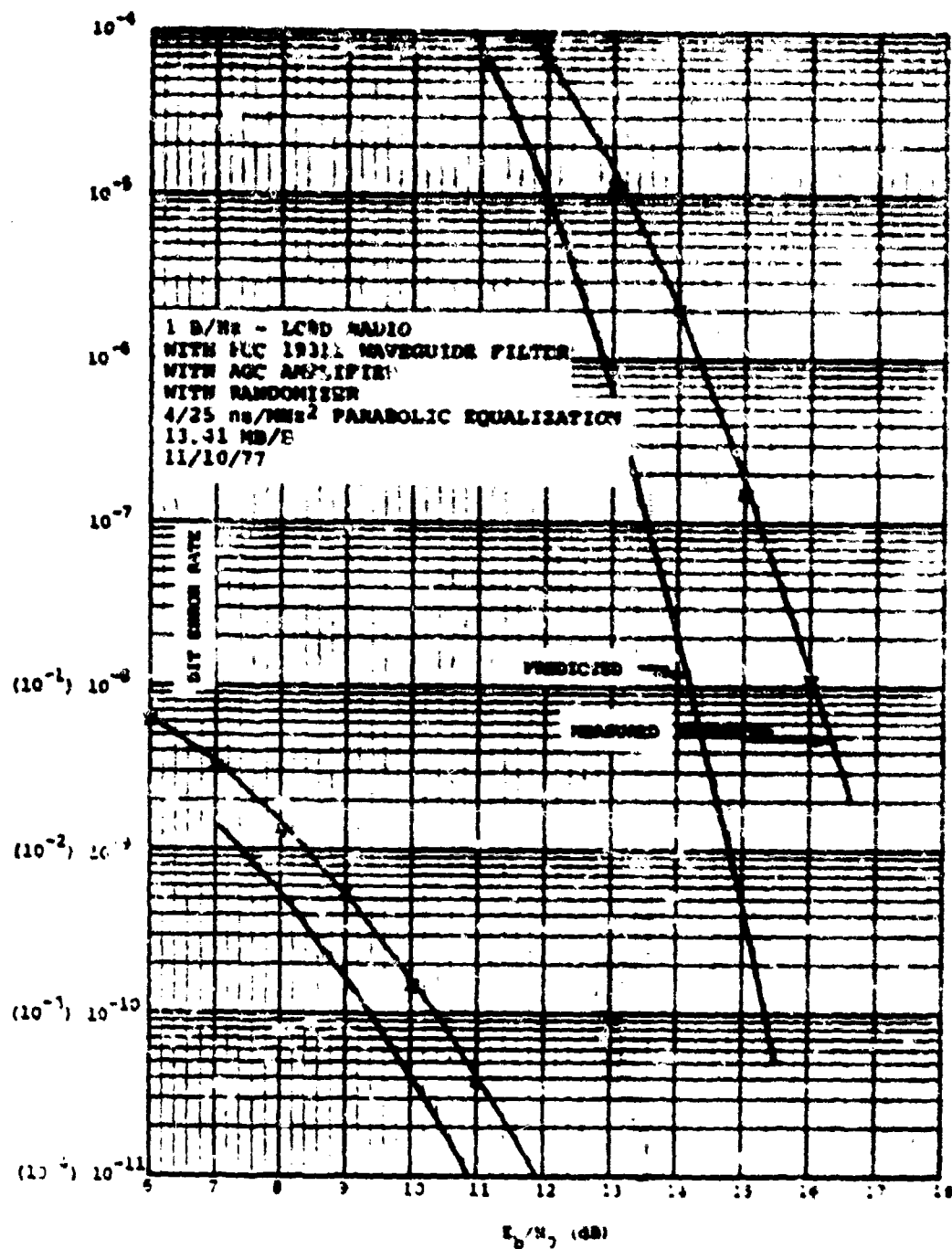
Figure 80. BER-1 B/Hz, LCBD Radio, With FCC 19311 Waveguide Filter, AGC Amplifier, Randomizer, and 4/25 ns/MHz^2 Parobolic Equalization

Tests were also run with radio noise as described in the previous paragraph. Figure 81 shows operation with an unequalized radio but with FCC 19311 filter, AGC, and randomizer. Figure 82 shows operation under the same conditions, but with 4/25 ns/MHz^2 parabolic group delay compensation. Performance appears to be better without equalization, but the difficulty in achieving repeatable measurements with this technique can easily account for apparent discrepancy. Both curves, however, show performance exceeding the design objecive of a 5×10^{-9} BER at an E_b/N_0 of 16 dB even though the randomizer was included when the data was taken.
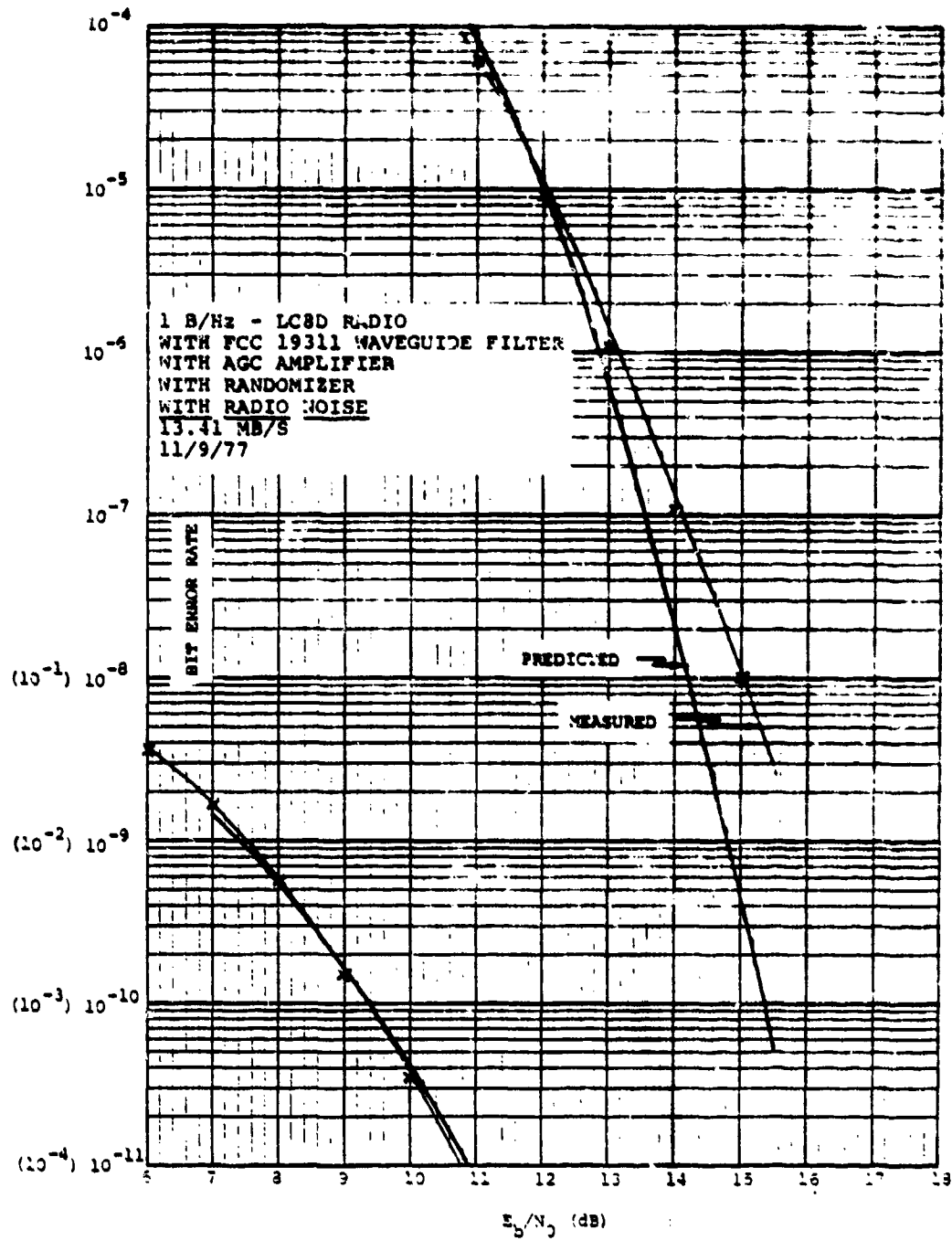
Figure 81. BER-1 B/Hz, LC8D Radio, With FCC 19311 Waveguide Filter, AGC Amplifier, Randomizer, and Radio Noise

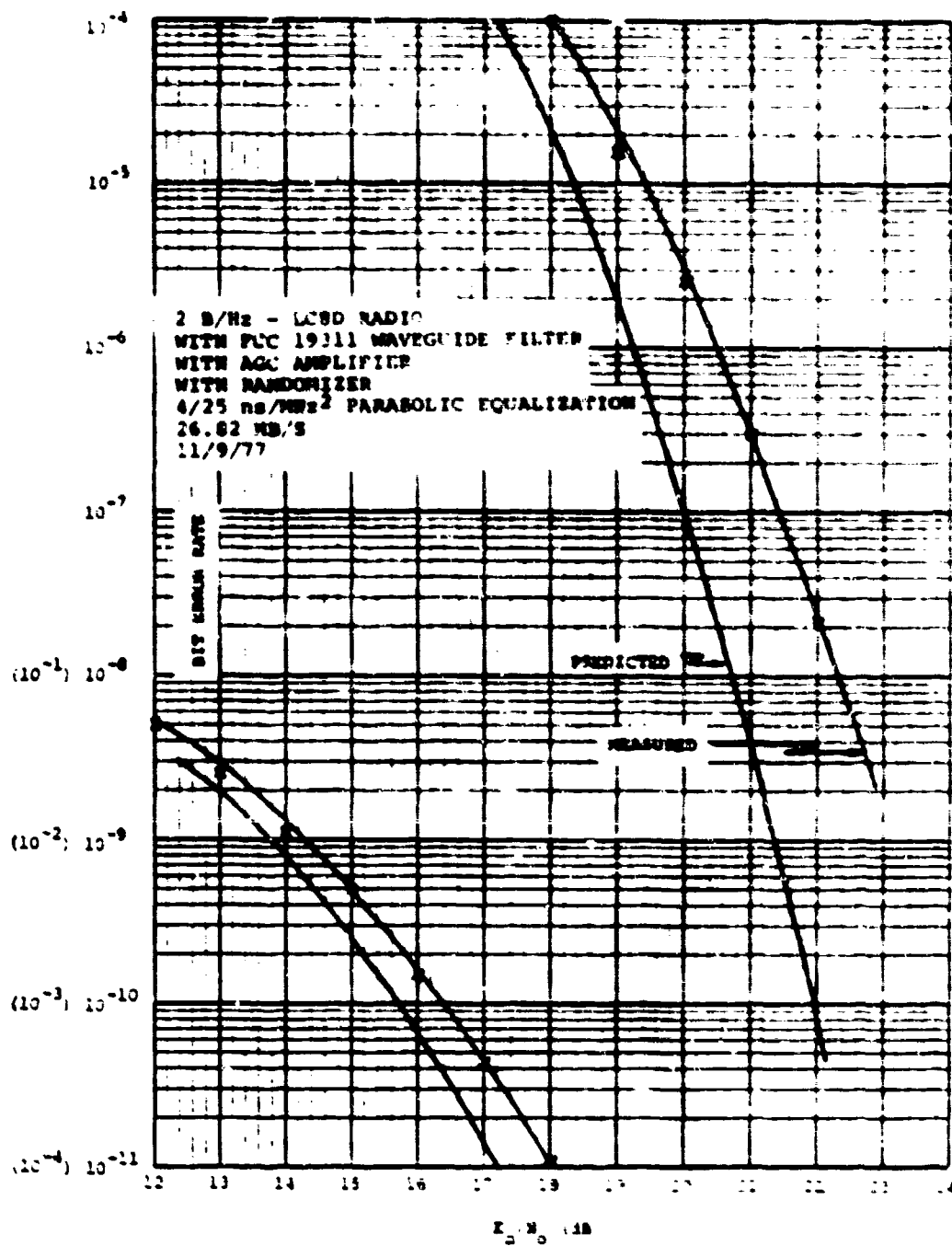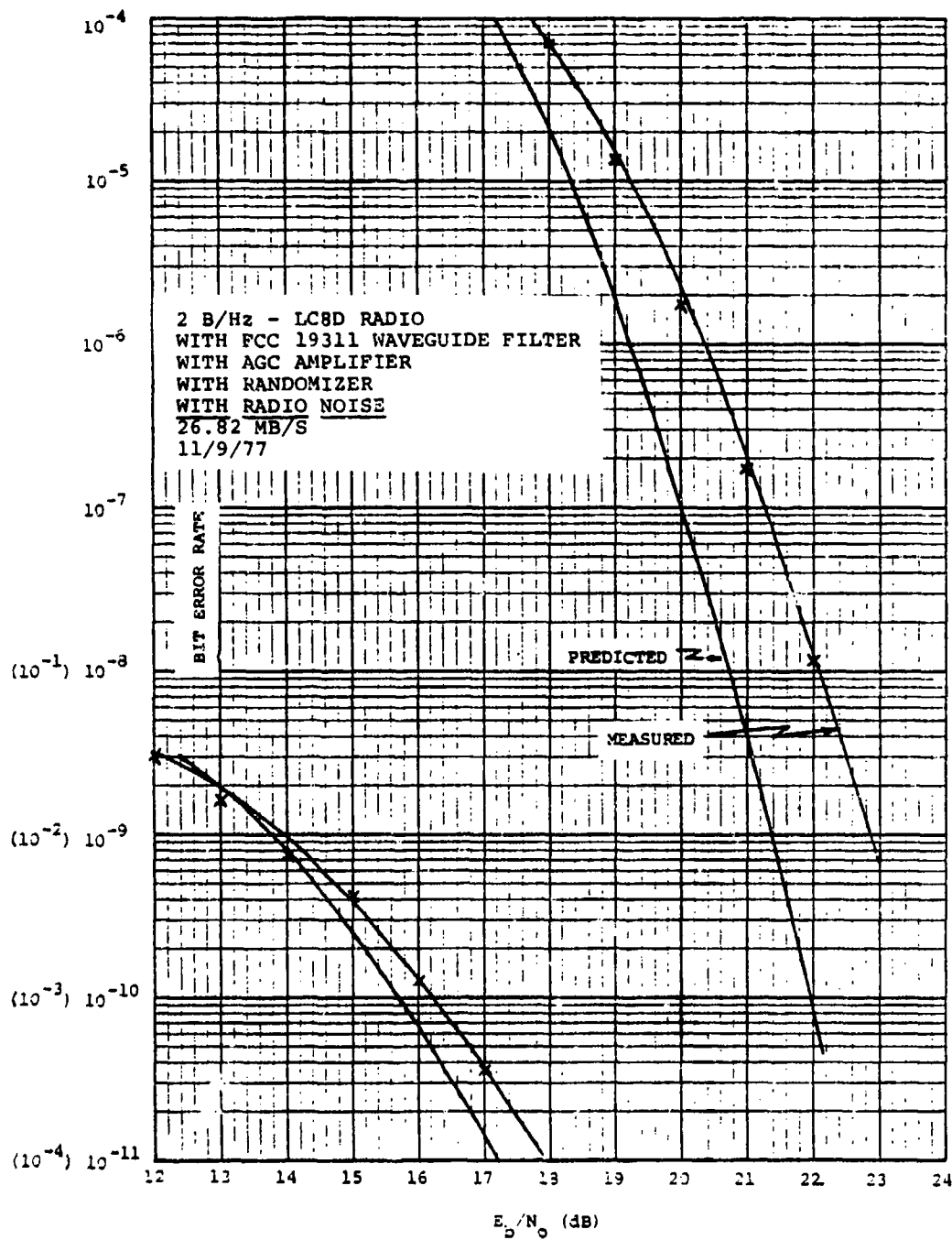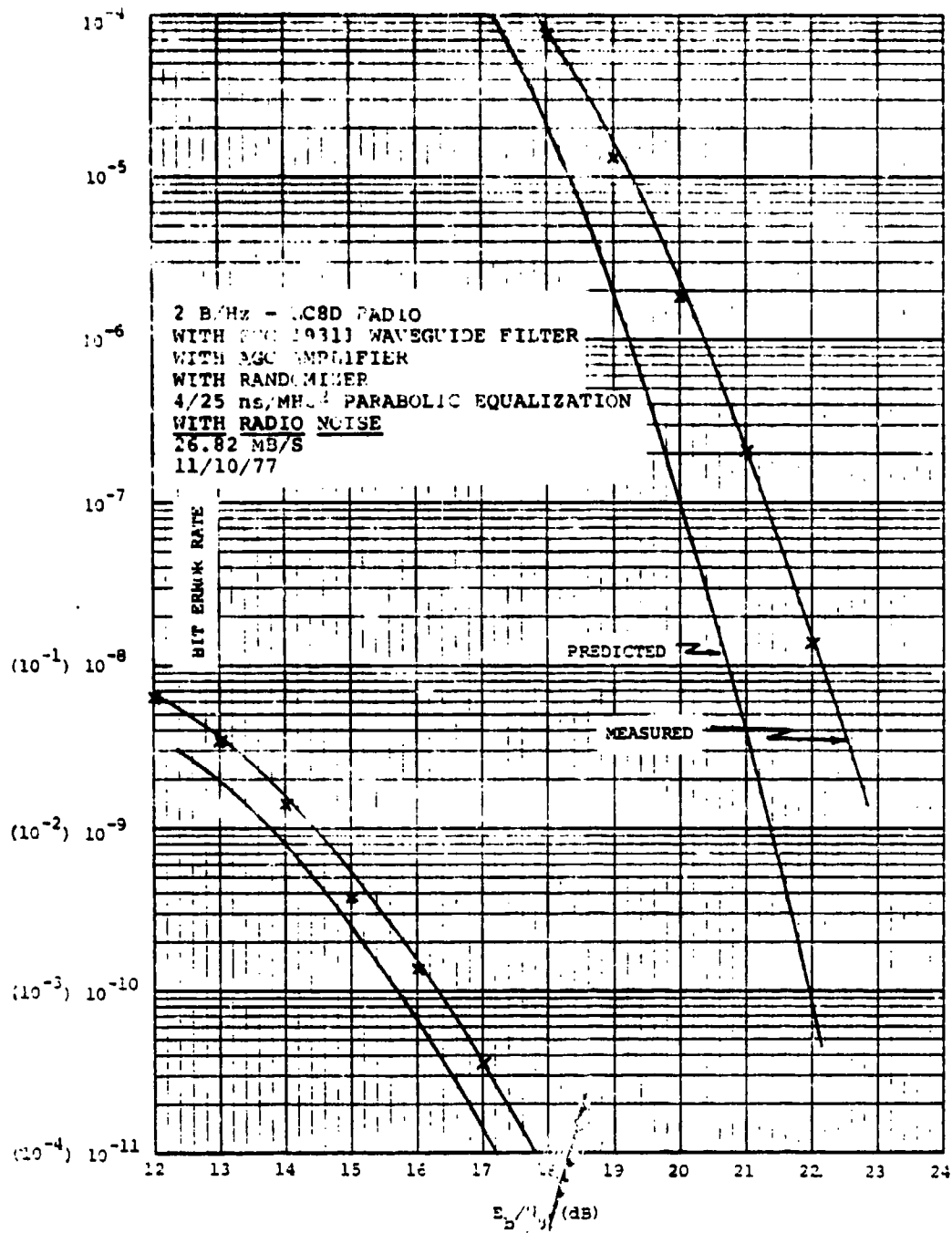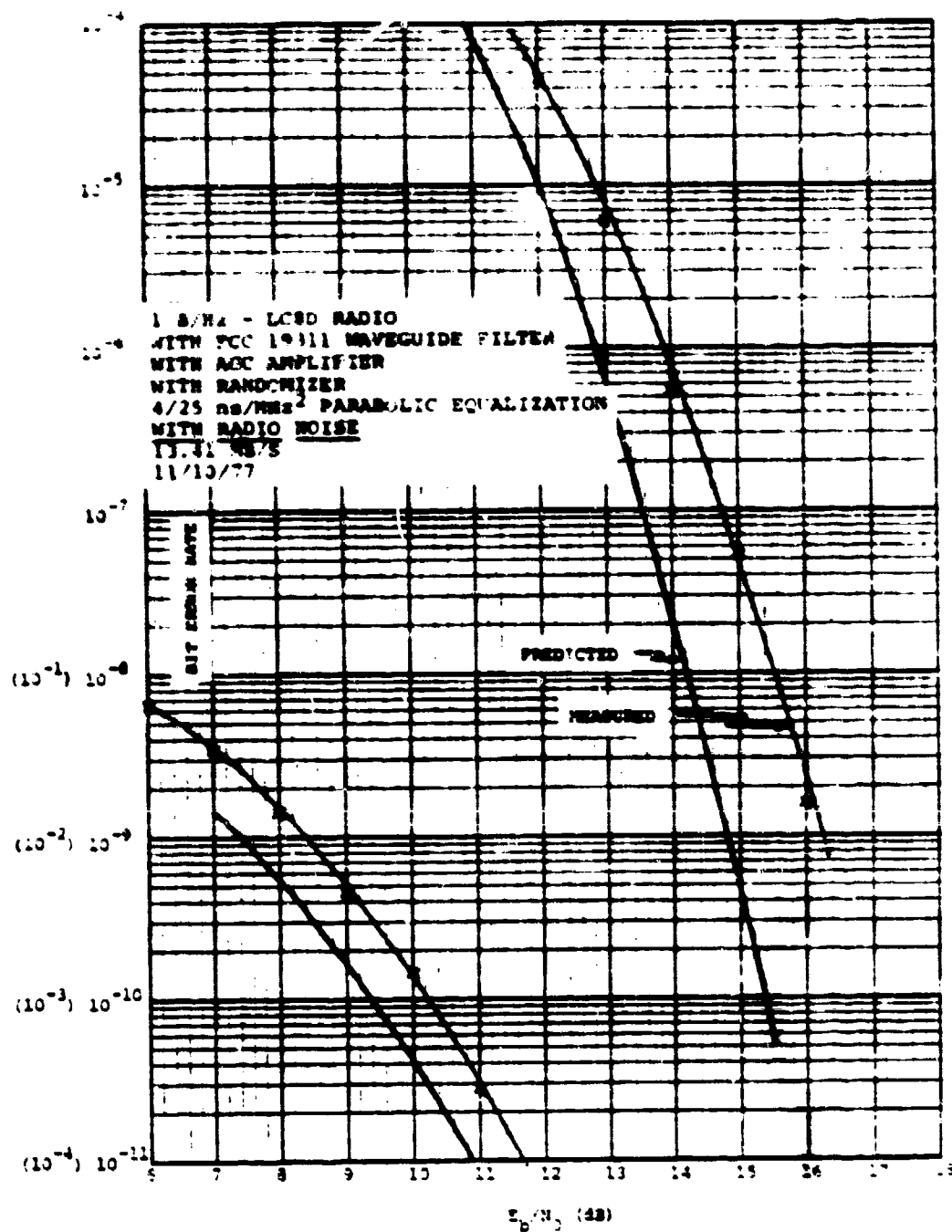Figure 82. BER-1 B/Hz, LC8D Radio, With FCC 19311 Waveguide Filter, AGC Amplifier, Randomizer, 4/25 ns/MHz² Parabolic Equalization With Radio Noise

SECTION 5.0

CONCLUSIONS

5.0   CONCLUSIONS

A practical experimental modem suitable for actual installation in hard-limiting line-of-sight microwave radio was constructed and successfully tested. The operational limitations evident in the previously constructed breadboard (see RADC-TR-76-117) have been eliminated. Performance is stable with time and rough handling. The additional features of an input multiplexer, data randomization, dual B/Hz capability, and compliance with FCC Docket 19311 have been included with only a slight degradation in bit error rate performance.

Total compliance with the spectral requirements of FCC Docket 19311 has been shown. The acquisition design objective of 20 ns for a 20 kHz IF frequency offset was met. The design objective of a bit error rate of 5×10^{-9} or less at an E_b/N_o of 16 dB when operating through the Philco Ford LC8D radio for a nominal 1 B/Hz spectral efficiency has been met within measurement accuracy. The randomizer/derandomizer has been shown not to degrade BER by more than a factor of three. Performance for a nominal 2 B/Hz spectral efficiency when operating through the LC8D radio misses the design objective of a bit error rate of 5×10^{-9} at an E_b/N_o of 22 dB by less than 0.6 dB with randomizer. Allowing for a factor of three improvement without randomizer, the design goal was missed by approximately 0.2 dB.

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APPENDIX A

FCC DOCKET 19311 SPECTRAL EFFICIENCY

APPENDIX A

FCC DOCKET 19311 SPECTRAL EFFICIENCY

The original goal on the previous breadboard unit was to provide a 2 B/Hz 99 percent spectral occupancy modem providing 10^{-7} error rate at E_b/N_o = 20 dB and this goal was achieved. FCC Docket 19311 employed in this study embodies a more stringent requirement on the radiated spectrum than simply 99 percent bandwidth spectral occupancy for digital signalling.

The FCC Docket 19311 requirement on digital modulation techniques is stated thus:

"For operating frequencies below 15 GHz, in any 4 kHz band, the center frequency of which is removed from the assigned frequency by 50 percent or more of the authorized bandwidth: As specified by the following equation but in no event less than 50 decibels.

$A = 35 + 0.8 \ (P-50) + 10 \ \log_{10}B$

(Attenuation greater than 80 decibels is not required.)

Where: A = attenuation (in decibels) below mean output power level

P = percent removed from the carrier frequency

B = authorized bandwidth in MHz."

Figure A-1 and A-2 show the implications of the 19311 requirement for the 4-ary signalling schemes of interest to Broadband Modem II for nominal 1 B/Hz operation and 2 B/Hz operation respectively. Both these signalling schemes assume a 14 MHz authorized bandwidth. The mod-index 0.125 signal actually has 99 percent spectral occupancy of 2.04 B/Hz and the mod-index 0.25 has 99 percent bandwidth 1.28 B/Hz. As can be seen, the mod-index 0.125 signal has up to an 18 dB problem in the spectrum side lobes relative to the 19311 requirement and the 0.25 signal has a 15 dB problem.

The study requirement was to find the most efficient means of reducing these side lobes to meet 19311. Two techniques were investigated; IF filtering and RF Waveguide filtering (see Paragraph 2.3.1 in body of report).

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Figure A-2. Comparison of Mod Index 0.125
4-ary FSK Spectrum with 19311 Requirement

Figure A-1. Comparison of Mod Index 0.25
4-ary FSK Spectrum with 19311 Requirement

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APPENDIX B

COMPUTER SIMULATION PROGRAM FOR BROADBAND MODEM II

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APPENDIX B

COMPUTER SIMULATION PROGRAM FOR BROADBAND MODEM II

A FORTRAN computer program was written to evaluate various filtering approaches considered in the study phase of this program. The computer program evaluates the approaches' spectra as well as the performance with the demodulator algorithm developed on the prior Broadband Modem contract.

Figure B-1 shows the system setup the computer program can handle. Any mod-index 4-ary FSK signal can be handled. The frequency
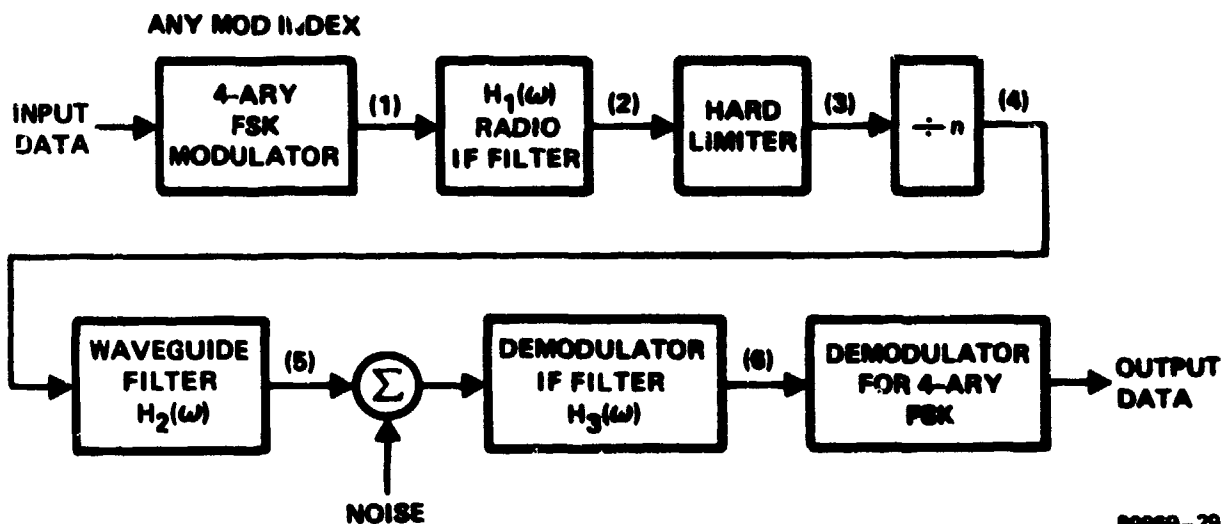
ANY MOD INDEX

Figure B-1. Situation That Computer Program Can Handle

divide-by-n block was included in order to evaluate approaches to FCC Docket 19311 compliance through filtering mod-index 1 signals and then divide-by-8 to produce mod-index 1/8 2 B/Hz signals. No significant advantage was found for this approach and it was discarded early in the study.

Referring to Figure B-1, a PN sequence is used to generate 4-ary FSK at point (1). A Fast Fourier Transform (FFT) routine is used to

compute the transform of the sequence. This transform is filtered by H_1 (which models any radio IF filters as well as any IF spectral shaping filters) to yield the transform of the signal at point (2). An inverse FFT yields time samples of the signal at (2). These samples are hard-limited to provide time samples of the signals at point (3). The phases are divided-by-n (if necessary) to yield time samples of the signal at point (4). Again, an FFT is performed on these samples to yield to Fourier transform of the signal at (4). The magnitude squared of this FFT is averaged over many sequences if IF filtering approach signal spectrum is desired. If a waveguide filter is included the FFT (4) is filtered by H_2 to yield Fourier transform of the signal at (5). Again, if spectrum at this point is desired, magnitude squared of the FFT at point (5) is averaged over many sequences. If not, the FFT at (5) is further filtered by H , the demod filter to yield Fourier transform of signal at point (6). This FFT is inverse transformed to yield time samples of the signal at (6). From these time samples the phase measurements that would be made by the demodulator are computed and these phases are fed to a separate program routine for computing average symbol error rate for the sequence. The noise is modelled analyt ically knowing E_b/N_o and effective noise bandwidth of the receive filter, H_3 - as opposed to Monte Carlo simulation.

This computer program was used to generate most of the results reported for Broadband Modem II. A listing of the program follows.

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```
C
C       THIS PROGRAM COMPUTES POWER SPECTRA OF  ARBITRARY MOD-INDEX
C       4-ARY FSK BY AVERAGING FAST FOURIER TRANSFORMS.
C       IT HAS CAPABILITY FOR DOING SO FOR FILTER/LIMITER COMBINATIONS
C       AS WELL AS FILTER AND NO LIMITER.
C
C       ALSO, PERFORMANCE OF THE PHASE DETECTOR ALGORITHM
C       DEVELOPED ON RADC 2 BITS/HERTZ CONTRACT CAN BE SIMULATED.
C
C       PROGRAMMER: BOB DAVIS, ATU, X5996
C
C
C
C
        DIMENSION AF(240)
        COMPLEX TSMP(512)
        COMPLEX CSMP(512),HT(512),ZVAR
        COMPLEX HR(512)
        DIMENSION ASPEC(512)
        DIMENSION WFN(512)
        DIMENSION PNODE(64)
        DIMENSION AMP(64)
        INTEGER SYMB(64)
        COMMON SYMB,PNODE,NSYM,AMP
        PI=3.14159
        IREG=15
C
C       READ IBBM EQUAL 1 IF BROADBAND MODEM PERFORMANCE DESIRED
C       IBBM EQUAL 0 IF SPECTRUM DESIRED
C
        READ(7,) IBBM
        WRITE(6,901) IBBM
901 FORMAT(" IBBM=",I2,"IBBM EQUALS 1 FOR B M PERFORMANCE")
C
C       ENTER NO. OF FOURIER XFRMS
C
        READ(7,) NFT
        IF(IBBM.EQ.1) NFT=1
        WRITE(6,902) NFT
902 FORMAT(" NO. OF SEQUENCES TO BE FFT'D = ,I4)
C
C       ENTER NO. OF 4-ARY SYMBOLS/XFORM (MUST E POWER OF TWO)
C
        READ(7,) NSYM
        WRITE(6,903) NSYM
903 FORMAT(" NO. OF SYMBOLS/SEQUENCE = ",I4
C
C       ENTER NO. OF SAMPLES/SYMBOL (MUST BE POWER OF TWO)
C
        READ(7,) NPS
        WRITE(6,904) NPS
904 FORMAT(" NO. OF SAMPLES/SYMBOL FOR FFT  ",I3)
C
```

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```
C     ENTER MOD/INDEX
C
      READ(7,) M
      WRITE(6,905) M
905 FORMAT(" FREQ. SPACING/SYMBOL RATE ("OD INDEX) =",F8.C)
C
C     ENTER FREQ. DIVIDE FACTOR
C
      READ(7,) NDIV
      WRITE(6,906) NDIV
906 FORMAT(" FREQ. DIVIDE FACTOR =",I4)
C
C     ENTER SYM RATE, SPECT. ANAL. BW IN SAME UNITS
C
      READ(7,) SR,ABW
      WRITE(6,907) SR,ABW
907 FORMAT(" SYMBOL RATE=",F10.3,/," SPECTR M ANALYZER BW =",F10.3)
      FACTOR=(ABW/SR)*NSYM
      IF(FACTOR.GT.1) STOP
C
C     ENTER INITIAL PHASE ANGLE
C
      READ(7,) THI
      WRITE(6,908) THI
908 FORMAT(" INITIAL PHASE ANGLE=",F10.3,"R DIANS")
      N=NSYM*NPS
C
C     COMPUTE XMIT FILTER FREQ. RESPONSE
C
      WRITE(6,909)
909 FORMAT(//,"DATA FOR TRANSMIT FILTER FOL OW")
      DLTAF=1./NSY"
      CALL TF(NX,DLTAF,HT)
C
C
C     READ "LIMIT" =1 IF HARD LIMITER AFTER T ANSMIT FILTER
C
      READ(7,) LIMIT
      IF(LIMIT.EQ.1) WRITE(6,912)
      IF(LIMIT.LE.1) WRITE(6,913)
912 FORMAT(//,"HARD LIMITER AFTER XMIT FILT R")
913 FORMAT(//,"NO LIMITER AFTER XMIT FILTER )
C
C     COMPUTE RECEIVE FILTER FREQ. RESPONSE
C
      WRITE(6,910)
910 FORMAT(/,"DATA FOR RECEIVE FILTER FOLL W")
      CALL TF(NX,DLTAF,HR)
C
C     COMPUTE KAISER WINDOWING FUNCTION
C
      BETA=7.
      CALL WINDOW(NX,BETA,WFN)
```

```
C
C       COMPUTE NORMALIZING FACTOR FOR WINDOW
C
        FNORM=0.
        DO 60 I=1,NX
   60   FNORM=FNORM+(WFN(I))**2
C
C       ZERO SPECTRUM AVGING. ARRAY
C
        DO 12 I=1,NX
   12   ASPEC(I)=0
C
C       READ TIMING DELTA IN SYMBOL TIMES
C
        READ(7,) DT
        WRITE(6,911) DT
  911   FORMAT(/,"TIMING DELTA IN SYMBOL TIMES= ,F10.4)
C
C       READ XMIT FREQUENCY DETUNING IN SYMBOL  ATES
C
        READ(7,) DETUNE
        WRITE(6,914) DETUNE
  914   FORMAT(//," XMITTER DETUNING IN SYMBOL  ATES=",F10.5)
C
C       START AVGING LOOP ON XFRMS
C
        DO 10 L=1,NFT
        THETA=THI
C
C       START LOOP ON SYMBOLS
C
        DO 2 J=1,NSYM
        IF(IBBM.NE.1) GO TO 502
C
C       SHIFT 6-BIT PN REGISTER TWICE FOR 4-ARY SYMBOL
C
        DO 1 I=1,2
        I1=IREG/32
        I2=MOD(IREG,2)
        I1=I1+I2
        I1=MOD(I1,2)
        IREG=2*IREG+I1
        IF(IREG.GT.63) IREG=IREG-64
    1   CONTINUE
  501   GO TO 503
  502   CONTINUE
C
C       SHIFT 15-BIT PN REG. TWICE FOR 4-ARY SY BOL
C
        DO 500 I=1,2
        NZ=IABS(IREG/16384-IREG+2*(IREG/2))
        IREG=2*IREG+NZ
        IF(IREG.GT.32767) IREG=IREG-32768
```

```
993 CONTINUE
503 CONTINUE
C
C       DETERMINE M-ARY SYMBOL (A)
C
        ISYM=MOD(IREG,M)
        SYM(J)=ISYM
        AA=ISYM-3
        IF(L.NE.NFT) GO TO 99
        IF(J.EQ.1) WRITE(6,600)
600 FORMAT(//,"SYMBOLS FOR LAST SEQUENCE FO LTW",//)
        WRITE(6,*) J,ISYM
 99 CONTINUE
C
C       COMPUTE SAMPLES OF LOG(PHASE) FO M THI  SYM
C
        L=(ERR(J-1))*NPS
        DO 3 K=1,NPS
        PHASE=THETA+(A*PI*K/NPS)*M
C
C       ACCOUNT FOR FREQUENCY DETUNING
C
        PHASE=PHASE+2.*PI*(DETUNE/NPS)*K
C
        I=L+INDEX+K
 4      CSMP(I)=CMPLX(COS(PHASE),SIN(PHASE))
C
C       MAINTAIN CONTINUOUS PHASE--END LOOP ON  YM
        PMODE(J)=PHASE*(180./PI)
 3      THETA=PHASE
C
C       COMPUTE FOURIER XFRM FOR THIS SEQ.
C
        CALL FOUR2(CSMP,NX,1,-1)
C
C       FILTER W/XMIT FILTER
C
        DO 30 I=1,NX
 30     CSMP(I)=CSMP(I)+HT(I)
C
C       INVERSE FFT
C
        CALL FOUR2(CSMP,NX,1,1)
C
C       HARD LIMIT & FREQUENCY DIVIDE (IF REQUI D)
C
        I=1+U
        DO 50 I=1,NX
        CSMP(I)=CSMP(I)/NX
        ZVAR=CLOG(CSMP(I))
        PHI=AIMAG(ZVAR)
        IF(I.EQ.1) PHIR=PHI
        IF(I.EQ.1) GO TO 50
```

```
      DLTAP=PHI-PHIR
      IF(DLTAP.GT.PI) INT=INT-1
      IF(DLTAP.LT.(-PI)) INT=INT+1
      PHIR=PHI
   50 PHI=PHI+2.*PI*INT
      PHI=PHI/NDIV
      IF(L.NE.NFT) GO TO 100
      IF(I.EQ.1) WRITE(6,444)
  444 FORMAT(//,"PHASES IN DEGREES AFTER XMIT FILTER FOLLOW",//)
      ISMP=MOD(I,NP3)
      IF(ISMP.NE.0) GO TO 100
      JEGPHI=PHI*(180./PI)
      WRITE(6,900) I,DEGPHI
  900 FORMAT(I4,F8.2)
  100 CONTINUE
      IF(LIMIT.NE.1) GO TO 101
      CSMP(I)=CMPLX(COS(PHI),SIN(PHI))
  101 CONTINUE
C
C
C     WEIGHT SAMPLES W/ KAISER WINDOWING FUNCTION
C     AND SAVE IN "TSMP" ARRAY
C
      TSMP(I)=CSMP(I)*WFN(I)
C
C
   90 CONTINUE
      IF(L.NE.NFT) GO TO 81
C
C     TAKE FFT
C
      CALL FOUR2(CSMP,NX,1,-1)
C
C
C     FILTER W/ RECEIVE FILTER
C
      DO 70 I=1,NX
      CSMP(I)=CSMP(I)/NX
   70 CSMP(I)=CSMP(I)*HR(I)
C
C     ACCOUNT FOR TIMING DELTA SHIFT
C
      DOMEG=2.*PI*DLTAF*DT
      DO 72 I=1,NX
      IFREQ=MOD((I+NX/2,NX)-NX/2-1
      ANG=-IFREQ*DOMEG
      ZVAR=CMPLX(COS(ANG),SIN(ANG))
   72 CSMP(I)=CSMP(I)*ZVAR
C
C     TAKE INVERSE FFT
C
      CALL FOUR2(CSMP,NX,1,1)
C
C     DETERMINE RECEIVED PHASE & PRINT
```

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```
C
      WRITE(6,300)
  300 FORMAT(/,"PHASES FROM RECEIVE FILTER FO LOW",/)
      INODE=0
      DO 80 I=NPS,NX,NPS
      ZVAR=CLOG(CSMP(I))
      PSI=AIMAG(ZVAR)
      PSI=PSI*(180./PI)
      INODE=INODE+1
      ETN=PSI-PNODE(INODE)
      IF(ETN.GT.180) ETN=ETN-360.
      IF(ETN.LT.(-180)) ETN=ETN+360.
      PNODE(INODE)=ETN
      AMP(INODE)=CABS(CSMP(I))
      WRITE(6,999) INODE,PSI,SYMB(INODE),ETN, MP(INODE)
  999 FORMAT(I3,F10.3,I2,F10.3,F10.3)
   80 CONTINUE
   91 CONTINUE
C
C     TAKE FFT OF WINDOWED TIME SAMPLES
C     FROM XMIT FILTER OUTPUT
C
      CALL FOUR2(TSMP,NX,1,-1)
C
C     ACCUMULATE FOURIER TRANSFORM SQUARED
C
      DO 15 I=1,NX
   15 ASPEC(I)=ASPEC(I)+(CABS(TSMP(I)))**2
C
C
C     END LOOP ON FFT,S
C
C     IF IBBM EQUALS 1 CALL ROUTINE FOR COMPU ING SYMBOL
C     ERROR RATE FOR THIS SEQUENCE
C
      IF(IBBM.NE.1) GO TO 10
      CALL BPMSER(SER)
   10 CONTINUE
C
C     READ BEGIN,END,INCREMENT
C
    5 READ(7,) NB,NE,INC
      JP = 120
      JO = 1
      MP = 2
      XMIN = 0.0
      XMAX = 120.0
      YMIN = -100.0
      YMAX = 0.0
      DO 40 I=NB,NE,INC
      A1=NFT
      A2=NX
      SPEC=FACTOR*ASPEC(I)/(A1*A2*FNORM)
```

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```
      AF(I) = I
   11 = I + 120
      AF(II) = 10. * ALOG10(SPL2)
      WRITE(16,11,AF(II)
51    CONTINUE
      WRITE(6,990)
990   FORMAT(1H1,36X,'SPECTRUM')
      CALL SPLOTH(NO,AF,NP,NP,U,G,XMAX,XMIN,Y AX,YMIN)
      STOP
      END
```

```
      SUBROUTINE TF(NX,DLTAF,H)
C
C       THIS SUBR. COMPUTES FILTER TRANS. FCN GIVEN POLES,ZEROS
C
      COMPLEX P(40),Z(40),WUG,PP,PZ,H(512)
      PI=3.14159265
C
C      READ NO. POLES, NO. ZEROS
C
      READ(7,) NP,NZ
      WRITE(6,900) NP,NZ
  900 FORMAT(" NO. POLES=",I4,"NO. ZEROS =",I )
C
C      READ BANDWIDTH MULT. FACTOR FOR POLES & ZEROS
C
      READ(7,) BW
      WRITE(6,901) PW
  901 FORMAT(" BANDWIDTH MULT. FACTOR FOR POLES & ZEROS =",F10.3)
C
      IF(NP.EQ.0) GO TO 30
C
C      READ COMPLEX POLES
C
      WRITE(6,902)
  902 FORMAT(" COMPLEX POLES FOLLOW : REAL,IM G.")
      DO 1 N=1,NP
      READ(7,) P(N)
      P(N)=BW*P(N)
      WRITE(6,) P(N)
    1 CONTINUE
   30 CONTINUE
      IF(NZ.EQ.0) GO TO 40
C
C      READ COMPLEX CZEROS
C
      WRITE(6,903)
  903 FORMAT(" COMPLEX ZEROS FOLLOW : REAL,IM G.")
      DO 2 N=1,NZ
      READ(7,) Z(N)
      Z(N)=BW*Z(N)
      WRITE(6,) Z(N)
    2 CONTINUE
   40 CONTINUE
C
C      READ UNITY GAIN FREQ.
C
      READ(7,) WG1
      WRITE(6,904) WG1
  904 FORMAT(" UNITY GAIN FREQ. =",F10.3)
      WUG=CMPLX(0.,WG1)
C
C      READ BW OVER WHICH GROUP DELAY IS TO BE AVGD. TO YIELD
C      TIME DELAY FOR THIS FILTER
```

```
C
      READ(7,) BWGD
      WRITE(6,905) BWGD
  905 FORMAT(" BW OVER WHICH GRP. DELAY AVGD. TO GET DELAY=+-",F10.3)
C
C     COMPUTE NORMALIZING FACTOR FOR GAIN
C
      PP=CMPLX(1.,0.)
      PZ=CMPLX(1.,0.)
      IF(NP.EQ.0) GO TO 4
      DO 3 N=1,NP
    3 PP=PP*(WUG-P(N))
    4 CONTINUE
      IF(NZ.EQ.0) GO TO 6
      DO 5 N=1,NZ
    5 PZ=PZ*(WUG-Z(N))
    6 GWUG=CABS(PZ/PP)
C
C     GWUG=GAIN AT DESIGNATED FREQ.
C
C     COMPUTE H(W) AT APPROPRIATE FREQS.
C     ALSO REMOVE DELAY THRU FILTER
C
      IREF=BWGD/DLTAF
      IF(IREF.EQ.0) IREF=1
      PHIDOT=0
      WRITE(6,200)
  200 FORMAT(//," IFREQ",5X," GAIN(DB)",5X," GROUP DELAY")
      DO 20 K=1,NX
      IFREQ=MOD(K+NX/2,NX)-NX/2-1
      W=DLTAF*IFREQ
      W=W+WG1
      WUG=CMPLX(0.,W)
      PP=CMPLX(1.,0.)
      PZ=CMPLX(1.,0.)
      IF(NP.EQ.0) GO TO 8
      DO 7 N=1,NP
    7 PP=PP*(WUG-P(N))
    8 CONTINUE
      IF(NZ.EQ.0) GO TO 10
      DO 9 N=1,NZ
    9 PZ=PZ*(WUG-Z(N))
   10 H(K)=(1./GWUG)*(PZ/PP)
C
C     DELAY CALCULATION FOLLOWS
C
C
      IF(IFREQ.EQ.0) PHIBGN=AIMAG(CLOG(H(K)))
      IF(IFREQ.EQ.0) PSHIFT=PHIBGN
      IF(IFREQ.EQ.0) GO TO 20
      IF(IABS(IFREQ).GT.IREF) GO TO 20
      IF(IFREQ.NE.(-IREF)) GO TO 80
      PHIBGN=AIMAG(CLOG(H(K)))
```

```
      GO TO 20
40 PHIEND=AIMAG(CLOG(H(K)))
      DELTA=PHIEND-PHIRGN
      IF(DELTA.GT.PI) DELTA=DELTA-2.*PI
      IF(DELTA.LT.(-PI)) DELTA=DELTA+2.*PI
      PHIDOT=PHIDOT-DELTA/(2.*IREF-1)
      PHIRGN=PHIEND
      GD=-DELTA/(2.*PI*DLTAF)
      GAIN=20.*ALOG10(CABS(H(K)))
      WRITE(6,) IFREQ,GAIN,GD
20 CONTINUE
      X=PHIDOT/(2.*PI*DLTAF)
      WRITE(6,100) X
100 FORMAT(" SYMBOLS TIMES DELAY = ",F8.2)
      PZ=CMPLX(COS(-PSHIFT),SIN(-PSHIFT))
      DO 50 K=1,NX
      IFREQ=MOD(K+NX/2,NX)-NX/2-1
      PP=CMPLX(COS(IFREQ*PHIDOT),SIN(IFREQ*PHIDOT))
      H(K)=PP*PZ*H(K)
50 CONTINUE
      RETURN
      END
```

```
      SUBROUTINE ACMODW(IX,BETA,UFN)
      DIMENSION UFN(1024)
      NIX=IX/2
      DO 1 N=1,NIX
      AN=N
      F=AN/ADX-1.
      F=1.-F**2
      F=BETA*SQRT(F)
1     UFN(N)=BI(F,0.001)
      RETURN
      END
```

```
      FUNCTION RI(Y,ACC)
      Z=(Y/2.)**2
      S=1.
      T=1.
      I=0
15    I=I+1
      R=Z/(I**2)
      T=T*R
      S=S+T
      IF(R-.95)25,25,15
25    SS=S*ACC-T*R/(1.-R)
      IF(SS)15,30,30
30    RI=S
      RETURN
      END
```

```
      SUBROUTINE FOUR2(DATA,NN,NDIM,ISIGN)
C     THE COOLEY-TUKEY FAST FOURIER TRANSFORM IN USASI BASIC FORTRAN
      DIMENSION DATA(2048),NN(3)
      TWOPI=6.2831853070
      IF(NDIM-1)700,1,1
    1 NTOT=2
      DO 2 IDEM=1,NDIM
      IF(NN(IDEM))700,700,2
    2 NTOT=NTOT*NN(IDEM)
C     MAIN LOOP FOR EACH DIMENSION
      NP1=2
      DO 600 IDEM=1,NDIM
      N=NN(IDEM)
      NP2=NP1*N
      IF(N-1)700,600,100
C     SHUFFLE DATA BY BIT REVERSAL, SINCE N=2 **K, AS THE SHUFFLING
C     CAN BE DONE BY INTERCHANGE, NO WORKING  RRAY IS NEEDED
  100 NP2HF=NP2/2
      J=1
      DO 160 I2=1,NP2,NP1
      IF (J-I2) 110,130,130
  110 I1MAX=I2+NP1-2
      DO 120 I1=I2,I1MAX,2
      DO 120 I3=I1,NTOT,NP2
      J3=J+I3-I2
      TEMPR=DATA(I3)
      TEMPI=DATA(I3+1)
      DATA(I3)=DATA(J3)
      DATA(I3+1)=DATA(J3+1)
      DATA(J3)=TEMPR
  120 DATA(J3+1)=TEMPI
  130 M=NP2HF
  140 IF(J-M)160,160,150
  150 J=J-M
      M=M/2
      IF(M-NP1)160,140,140
  160 J=J+M
C     LENGTH TWO IF NEETIDDLE FACTOR W=EXP(IS GM*2*PI*
C     AND REPEAT FORT(-1)*CONJUGATE(W).
      NP1T=NP1+NP1
      IPAR=N
  310 IF(IPAR-2)350,330,320
  320 IPAR=IPAR/4
      GO TO 310
  330 DO 340 I1=1,NP1,2
      DO 340 K1=I1,NTOT,NP1TW
      K2=K1+NP1
      TEMPR=DATA(K2)
      TEMPI=DATA(K2+1)
      DATA(K2)=DATA(K1)-TEMPR
      DATA(K2+1)=DATA(K1+1)-TEMPI
      DATA(K1)=DATA(K1)+TEMPR
  340 DATA(K1+1)=DATA(K1+1)+TEMPI
```

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```
350  WMAX=NP1
360  IF(NMAX-NP2HF)370,600,600
370  LMAX=MAX0(NP1TW,NMAX/2)
     IF(NMAX-NP1)405,415,5A
380  THET=-TWOPI*FLOAT(LN-1)/FLOAT(4*NMAX)
     IF(ISI-N)403,390,390
390  THETA=-THET
400  WR=COS(THETA)
     WI=SIN(THETA)
     WSTPR=-2.*WI*WI
     WSTPI=2.*WR*WI
405  DO 570 L=NP1,LMAX,NP1TW
     I=L
     IF (NMAX-NP1) 420,420,410
410  W2R=WR*WR-WI*WI
     W2I=2.*WR*WI
     W3R=W2R*WR-W2I*WI
     W3I=W2R*WI+W2I*WR
420  DO 520 II=1,NP1,2
     KMIN=IPAR*I+1
     IF (NMAX-NP1) 430,430,440
430  KMIN=I1
440  KDIF=IPAR*NMAX
450  KSTEP=4*KDIF
     DO 520 K1=KMIN,NTOT,KSTEP
     K2=K1+KDIF
     K3=K2+KDIF
     K4=K3+KDIF
     IF (NMAX-NP1) 460,460,480
460  U1R=DATA(K1)+DATA(K2)
     U1I=DATA(K1+1)+DATA(K2+1)
     U2R=DATA(K3)+DATA(K4)
     U2I=DATA(K3+1)+DATA(K4+1)
     U3R=DATA(K1)-DATA(K2)
     U3I=DATA(K1+1)-DATA(K2+1)
     IF (ISI) 465,475,75
470  U4R=DATA(K3+1)-DATA(K4+1)
     U4I=DATA(K4)-DATA(K3)
     GO TO 510
475  U4R=DATA(K4+1)-DATA(K3+1)
     U4I=DATA(K3)-DATA(K4)
     GO TO 510
     T2R=W2R*DATA(K2)-W2I*DATA(K2+1)
     T2I=W2R*DATA(K2+1)+W2I*DATA(K2)
     T3R=WR*DATA(K3)-WI*DATA(K3+1)
     T3I=WR*DATA(K3+1)+WI*DATA(K3)
     T4R=W3R*DATA(K4)-W3I*DATA(K4+1)
     T4I=W3R*DATA(K4+1)+W3I*DATA(K4)
     U1R=DATA(K1)+T2R
     U1I=DATA(K1+1)+T2I
     U2R=T3R+T4R
     U2I=T3I+T4I
     U3R=DATA(K1)-T2R
```

```
      U3I=DATA(K1+1)-T2I
      IF (ISIGN) 490,500,500
490   U4R=T3I-T4I
      U4I=T4R-T3R
      GO TO 510
500   U4R=T4I-T3I
      U4I=T3R-T4R
510   DATA(K1)=U1R+U2R
      DATA(K1+1)=U1I+U2I
      DATA(K2)=U3R+U4R
      DATA(K2+1)=U3I+U4I
      DATA(K3)=U1R-U2R
      DATA(K3+1)=U1I-U2I
      DATA(K4)=U3R-U4R
520   DATA(K4+1)=U3I-U4I
      KMIN=4*(KMIN-I1)+I1
      KDIF=KSTEP
      IF (KDIF-NP2) 450,530,530
530   CONTINUE
      M=MMAX-M
      IF (ISIGN)540,550,550
540   TEMPR=WR
      WR=-WI
      WI=-TEMPR
      GO TO 560
550   TEMPR=WR
      WR=WI
      WI=TEMPR
560   IF (M-LMAX) 565,565,410
565   TEMPR=WR
      WR=WR*WSTPR-WI*WSTPI+WR
570   WI=WI*WSTPR+TEMPR*WSTPI+WI
      IR=3-IPAR
      LMAX=MMAX+MMAX
      GO TO 360
C
C     END OF LOOP OVER EACH DIMENSION
C
600   NP1=NP2
700   RETURN
      END
```

```
      SUBROUTINE NOISE4(ASLM)
      DIMENSION MOVE(16),LU(16),ICHB(16),LHT(16),ICHBT(16)
      INTEGER TF(16)
      INTEGER SYMB(16)
      DIMENSION PHO(C(16)
      DIMENSION AMP(16)
      COMMON SYMB,MODE,SYM,AMP
      DIMENSION T(19)
      DIMENSION P(65,11)
      DIMENSION PSEQ(19)
      DIMENSION LEVEL(17)
      PI=3.1415
C
C     READ RCVR FILTER NOISE BW IN BIT RATES
C
      READ(7,) RFNB
      WRITE(6,900) RFNB
  900 FORMAT(" RCVR. FILTER NOISE BW IN BIT R TES=",F10.3)
C
C     READ EB/NO IN DB
C
      READ(7,) EBNO
      WRITE(6,901) EBNO
  901 FORMAT(" EB/NO IN DB =",F10.3)
C
C     COMPUTE S/N RATIO OUT OF RCVR FLTR
C
      SNR=(10.**(0.1*EBNO))/RFNB
C
C     COMPUTE NOISE-CAUSED PHASE JITTER IN DE S. RMS
C
      PJIT=(SQRT(1./(2.*SNR)))*(180./PI)
      WRITE(6,902) PJIT
  902 FORMAT(" NOISE CAUSED PHASE JITTER IN D FS. RMS=",F10.3)
C
C     READ LOOP-CAUSED SYSTEMATIC JITTER IN D GS. RMS
C
      READ(7,) SJIT
      WRITE(6,903) SJIT
  903 FORMAT(" LOOP-CAUSED JITTER IN DEGS. RM =",F10.3)
C
C     COMPUTE TOTAL RMS PHASE JITTER IN DEGS.
C
      TJIT=SQRT(PJIT**2+SJIT**2)
      WRITE(6,904) TJIT
  904 FORMAT(" TOTAL RMS PHASE JITTER IN DEGS  RMS=",F10.3)
C
C     READ THRESHOLD & NODE SPACING IN DEGREE
C
      READ(7,) TH,SPN
      WRITE(6,905) TH,SPN
  905 FORMAT(" THRESHOLD SPACING IN DEGS,=",F 0.3,"NODE SPACING=",F10.3)
C
```

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```
C     COMPUTE LOCATION OF EACH THRESHOLD
C
      T(1)=-SPN/2.-2.*TH
      T(2)=-SPN/2.-TH
      T(3)=-SPN/2.
      T(4)=-SPN/2.+TH
      T(5)=-SPN/2.+2.*TH
      T(6)=SPN/2.-2.*TH
      T(7)=SPN/2.-TH
      T(8)=SPN/2.
      T(9)=SPN/2.+TH
      T(10)=SPN/2.+2.*TH
C
C     READ NO. OF PHASES TO BE DISREGARDED ON EACH END OF SET
C     COMPUTED BY FFT ROUTUNE ( THIS IS TO AV ID TRANSIENTS)
C
C
      READ(7,) NDIS
      WRITE(6,906) NDIS
  906 FORMAT(" NO. OF PHASES FROM ENDS OF FFT SEQ. DISREGARDED=",I4)
C
C     COMPUTE TOTAL NO. OF PHASES LEFT TO BE  ONSIDERED
C
      NS=NSYM-2*NDIS
C     REARRANGE SEQUENCE DISREGARDING ENDS
C
      WRITE(6,907)
  907 FORMAT(" SYMBOL,DEGS. ERROR TO NODE IN  EQ. USED GET SER FOLLOW")
      DO 1 I=1,NS
      IX=I+NDIS
      PNODE(I)=PNODE(IX)
      SYMB(I)=SYMB(IX)
      AMP(I)=AMP(IX)
      WRITE(6,) SYMB(I),PNODE(I),AMP(I)
    1 CONTINUE
C
C     CALCULATE PROB. OF EACH OF 11 REGIONS F R EACH SYMBOL
C
      DO 2 N=1,NS
      V=(T(1)-PNODE(N))/TJIT
      V=AMP(N)*V
      P(N,1)=1.-Q(V)
      V=(T(10)-PNODE(N))/TJIT
      V=AMP(N)*V
      P(N,11)=Q(V)
      DO 3 L=2,10
      L1=L-1
      VU=(T(L)-PNODE(N))/TJIT
      VU=AMP(N)*VU
      VL=(T(L1)-PNODE(N))/TJIT
      VL=AMP(N)*VL
    3 P(N,L)=Q(VL)-Q(VU)
    2 CONTINUE
```

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```
C
C      MENS NO. OF PHASES USED IN ALGORITHM TO MAKE FINAL DECISIONS
C
       READ(7,) NP
       WRITE(6,  )
310    FORMAT( NO. OF           ALGORITHM TO  ARE FINAL DECS.=",I2)
       NPR2=NP*2
       LOC1=NP+NP
       LOC2=NP+NP+1
C
C      READ SEQUENTIAL PROBABILITY LO         PPR R THRESHOLDS
C
       READ(7,) THRESM,TP
       WRITE(4,999) THRESM,TP
310    FORMAT( LOWER SEQ. PROB. THRESH.=",E10 3,"UPPER THRESH.=",E10.3)
C
C      COMPUTE SHIFT STATE
C
       MENOP=SHIFT
C
C      INITIALIZE ...T. FOR SEQUENCE ISOLATION   ROUTINE
C
       DO 13 L=1,18
13     PSEQ(L)=1.
       DO 11 L=1,17
12     LEVEL(L)=1
       J=NP-1
       J=NP-6
       L=NPU
       JE=NP3
C
C      SEQUENCE ISOLATION ROUTINE FOLLOWS
C
       ISEQ=NPR+JP+2
       L=LC(JP)+1
       P=PSEQ(JP)*P(JP+1)*PS(L)
       IF(TP.LT.THRESM) GO TO 3
       JPP=JPP+1
       PSEQ(JPP)=TP
       IF(JPP.LE.NP) GO TO 6
C
C      SEQUENCE HAS BEEN ISOLATED
C      DECODE ROUTINE GOES HERE
C
C      IF SEQ. PROB. IS GREATER THAN UPPER THRESHOLD,SKIP DECODE
C      BECAUSE ERROR IS NOT MADE ANYWAY THE NO E  )
       IF(TP.GT.UT+1) GO TO 32
C
C      DECODE ROUTINE FOLLOWS
C
C      TENTATIVE PHASE DECISION PASS
C      FIVE LOOP IDENTIFIES BLOCK OF 2 RETAINED PHASES
```

```
      DO 21 J=1, ITO
      LEV=LEVEL(J)
      IF(LEV.EQ.11) MOVE(J)=1
      IF((LEV.GE.6).AND.(LEV.LT.11)) MOVE(J)=
     *1
      IF((LEV.LT.6)) MOVE(J)=-1
   21 CONTINUE
C
C     TENTATIVE FREQUENCY DECISIONS
C     TENTATIVE FRED. = LINE BETWEEN 2 BOTTOM RETAINED PHASES
C
      DO 22 J=2,ITO
      J1=J-1
      JSYM=NPEF+J
      IF(J)=SYMB(JSYM)+MOVE(J)-MOVE(J1)
   22 CONTINUE
C
C     FIRST PASS, UPPER/LOWER DECISION, CHANG MIND BITS
C
      DO 23 J=3,ITO
      J1=J-1
      J2=J-2
      LU(J2)=0
      ICHG(J2)=0
      LEV=LEVEL(J1)
      IF((LEV.EQ.11).OR.(LEV.EQ.6).OR.(LEV.EQ 11) GO TO 23
      ITM=TF(J)-TF(J1)
      IF(MOVE(J1).EQ.0) LCOMP=6+ITM
      IF(MOVE(J1).EQ.(-1)) LCOMP=3+ITM
      IF(LEV.NT.LCOMP) LU(J2)=1
      IF(LEV.EQ.LCOMP) ICHG(J2)=1
      L=LCOMP+1
      IF(LEV.EG.L) ICHG(J2)=1
   23 CONTINUE
C
C     LU(1) THRU LU(ITO-2) CONTAIN UPPER/LOWE DECISIONS
C     ICHG(1) THRU ICHG(ITO-2) CONTAIN "CHANG MIND" BITS
C
      L2=ICHG(LOC1)+ICHG(LOC2)
      IF(L2.NE.0) GO TO 30
      L2=LU(LOC2)
      L1=LU(LOC1)
      L(12)=L2
      L(11)=L1
      GO TO 31
C     SUCCESSIVE PASSES FOLLOW
C
   30 DO 24 IP=2,NUP
      ICTR=NTO-2+IP
      DO 25 J=1, ICTR
      J1=J+1
      IF(ICHG(J1).EQ.1) GO TO 26
      L(J1)=LU(J1)
      ICHG(J1)=ICHG(J1)
```

```
      GO TO 25
   26 J2=J+2
      IDLTA=LU(J)+LU(J2)-1
      LUT(J)=LU(J1)
      ICHGT(J)=ICHG(J1)
      IF((LUT(J).EQ.0).AND.(IDLTA.EQ.(-1))) LUT(J)=1
      IF((LUT(J).EQ.1).AND.(IDLTA.EQ.1)) LUT( )=0
   25 CONTINUE
      DO 27 J=1,NDIM
      LU(J)=LUT(J)
   27 ICHG(J)=ICHGT(J)
   24 CONTINUE
C
C     FINAL FREQUENCY DECISION FOLLOWS
C
   31 IRF=NREF+NOP+2
      ITFR=NOP+2
      FF=TF(ITFR)+LU(2)-LU(1)
      IF(FF.GT.3) FF=3
      IF(FF.LT.0) FF=0
      ISREF=SYMB(IRF)
      IERROR=0
      IF(FF.NE.ISREF) IERROR=1
C
C     AT THIS POINT "IERROR" =0 IF NO ERROR F R ISOLATED SEQUENCE
C                   "IERROR" =1 IF A FREQUENC  ERROR IS MADE
C
      IF(IERROR.EQ.1) SER=SER+TP
C
C     END OF DECODE ROUTINE
C
C
C
C
   32 CONTINUE
      ISO=ISO+1
      JREF=NTD
    5 LEVEL(JREF)=LEVEL(JREF)+1
      LTEST=LEVEL(JREF)
      IF(LTEST.LE.11) GO TO 4
      LEVEL(JREF)=1
      JREF=JREF-1
      IF(JREF.GT.0) GO TO 5
    6 JREF=NREF+1
      ASER=SER/NREF
      WRITE(6,910) JREF,ISO,ASER
  910 FORMAT(" SYMB. # DECODED=",I3,"NO. SEQS  ISOLATED=",I8,"AVG. SER S
     10 FAR=",E10.2)
      ISO=0
      IF(NREF.GT.NREND) GO TO 7
      JREF=1
      PSEQ(1)=1.
      GO TO 4
    7 CONTINUE
```

```
      FUNCTION Q(X)
      AX=ABS(X)
      IF(AX.GT.8) P=0.
      IF(AX.GT.8) GO TO 10
      T=1.0/(1.0+.2316419*AX)
      F=0.3989423*EXP(-X*X/2.0)
      P=F*T*((((1.330274*T-1.821256)*T+1.781478)*T-
     10.3565638)*T+.3193815)
 10   IF(X) 20,30,30
 20   P=1.0-P
 30   Q=P
      RETURN
      END
```

APPENDIX C

TEST PLAN

APPENDIX C

TEST PLAN

1.0   SCOPE

This plan describes a test program for the Broadband Digital
Modem. The tests will be conducted at RADC and at HARRIS Electronic
Systems Division (Harris ESD) in Melbourne, Florida.

2.0   OBJECTIVE

The overall objective is to characterize the critical
performance parameters of the modem. Specific tests include:

    a. Spectral Efficiency

    b. BER versus E_b/N_0

    c. Acquisition

3.0   MODEM DESCRIPTION

The Broadband Modem II was developed to improve the available
bandwidth efficiency in digital Line-of-Sight microwave systems. The
primary performance objective is a 5×10^{-9} BER at an E_b/N_0 of 22 dB
at a data rate of 26.82 Mb/s. The unit provides a bandwidth efficiency of
2 B/Hz of RF bandwidth and interfaces at 70 MHz with hard limiting radio
systems. The modem is also configured to operate at a bandwidth efficiency
of 1 B/Hz of RF bandwidth. The primary performance objective for this mode
of operation is 5×10^{-9} BER at an E_b/N_0 of 16 dB at a data rate of
13.41 Mb/s.

3.1   Technique Description

The modulation technique is continuous phase, 4-ary FSK with a
modulation index of 1/8 (i.e., the four tones are spaced at 1/8th the

symbol rate frequency intervals). The modulator is shown conceptually in Figure C-1. The demodulator employs coherent detection and multisymbol observation techniques to achieve the required performance. The demodulator is shown in Figure C-2.
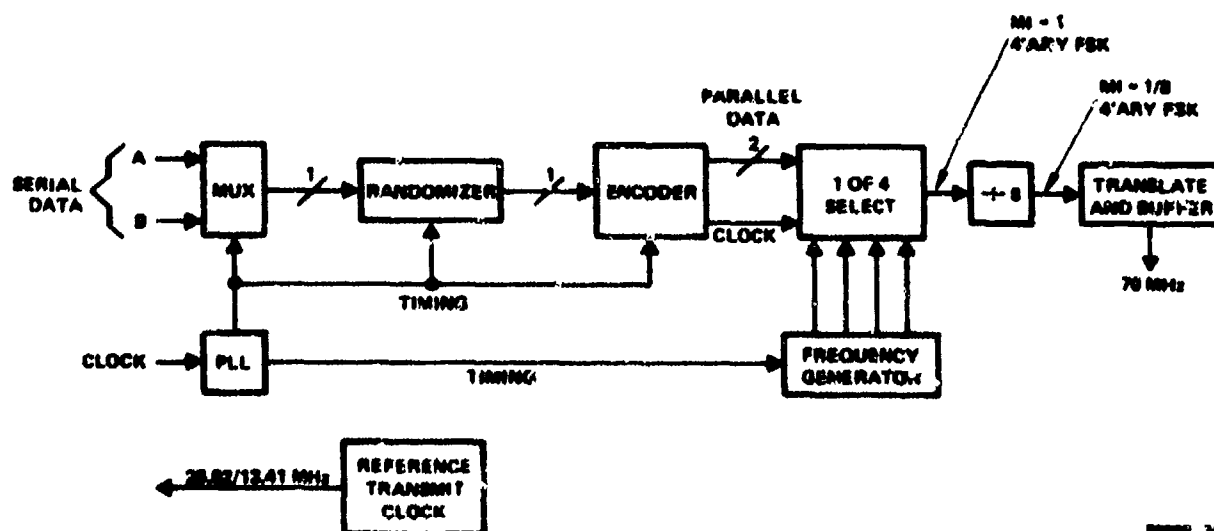

Figure C-1. Modulator Conceptual Block Diagram

3.2   Hardware Description

The modulator and demodulator are individually packaged in 19-inch chassis with integral power supplies. On the transmit side, the modulator provides a transmit clock and accepts either a single bit rate data stream and associated timing or 2-1/2 bit rate data streams to be MUXed together and associated timing. The transmit clock automatically adjusts rate for the chosen mode of operation. All digital interfaces are 75-ohm, unbalanced, bipolar interfaces. The modulated, 70 MHz carrier is outputted at +1 dBm level to the radio. The demodulator accepts a +1 dBm, 70 MHz signal from the radio and outputs data and synchronous timing. The modulator's 20-stage randomizer can be configured to operate as a

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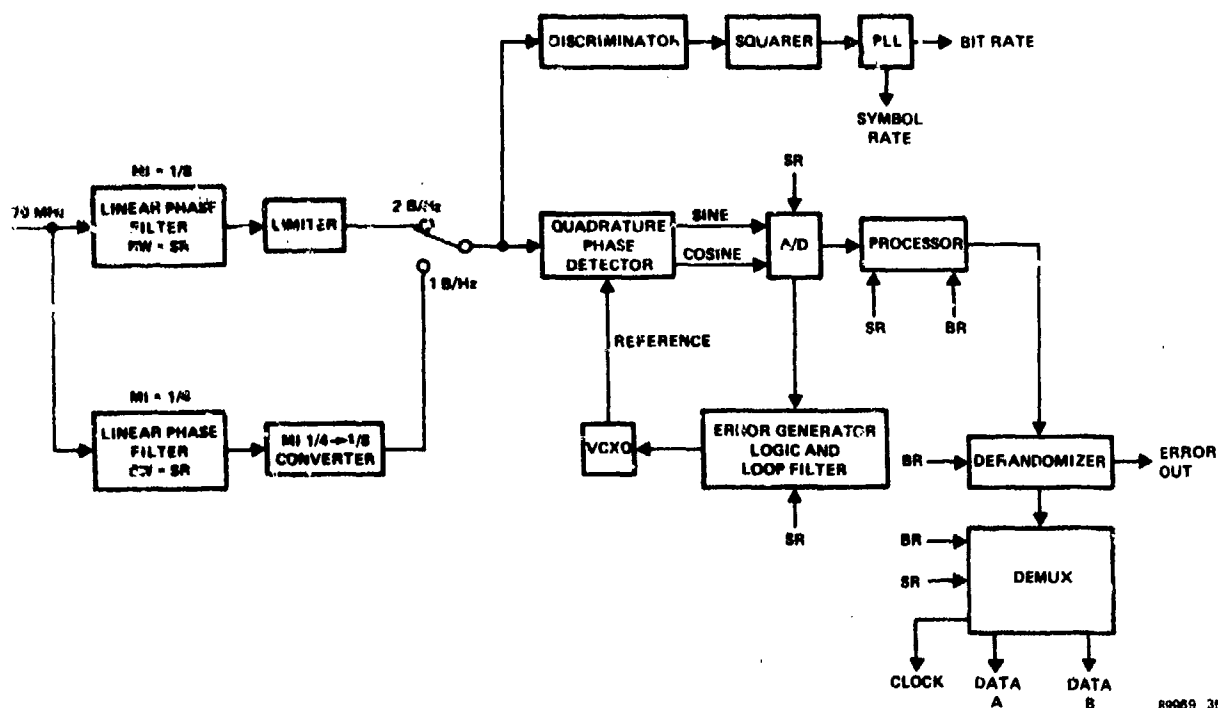
Figure C-2. Demodulator Conceptual Block Diagram

pseudorandom sequence generator which is decoded in the demodulator to
provide a bit error output. This may be monitored by an external frequency
counter to determine BER without the use of external data generators and
error detectors. The use of the randomizer/derandomizer degrades BER by a
factor of three. This is reflected in the bit error output on the
demodulator. For convenience, BER tests may also be performed with the

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randomizer and derandomizer by-passed. This may be accomplished by a simple internal wiring change in both boxes. An external data source and error counter are then required.

4.0 TEST PROGRAM

The test program includes tests at Harris ESD in Melbourne, Florida, and at RADC. The in-plant tests are designed to provide a performance baseline from which to interpret results from the later radio and link tests and to verify the characteristics of various internal parameters. Most of these tests are performed with the modem looped back at 70 MHz with additive thermal noise. In order to meet the spectral efficiency requirements of FCC Docket 19311 an RF waveguide filter at 8.075 GHz is to be employed. Although final performance verification of this technique must await installation of the filter in the LC8D radio, initial tests at Harris employing an upconversion from 70 MHz to 8.075 GHz and back down to 70 MHz with thermal noise added to the IF input to the demodulator will be performed. The RADC tests include both back-to-back tests with the radio simulator and link tests utilizing the Stockbridge radio.

4.1 In-Plant Tests

The test configuration for in-plant tests is shown in Figure C-3. A diagram of the up/downconverter for waveguide filter tests is shown in Figure C-4.

4.1.1 Spectral Efficiency

The objective of this test is to demonstrate that the output of the modulator upconverted to 8.075 GHz and filtered with the supplied waveguide filter meets FCC Docket 19311 requirements. A computer generated spectral mask, plotting energy in 4 kHz bandwidth versus offset frequency from center, is available. The actual transmit spectrum is plotted using a spectrum analyzer set for a 3 kHz IF bandwidth. The absolute level is calibrated by observing the difference in spectral height at center frequency between an unmodulated tone and a randomly modulated signal. If
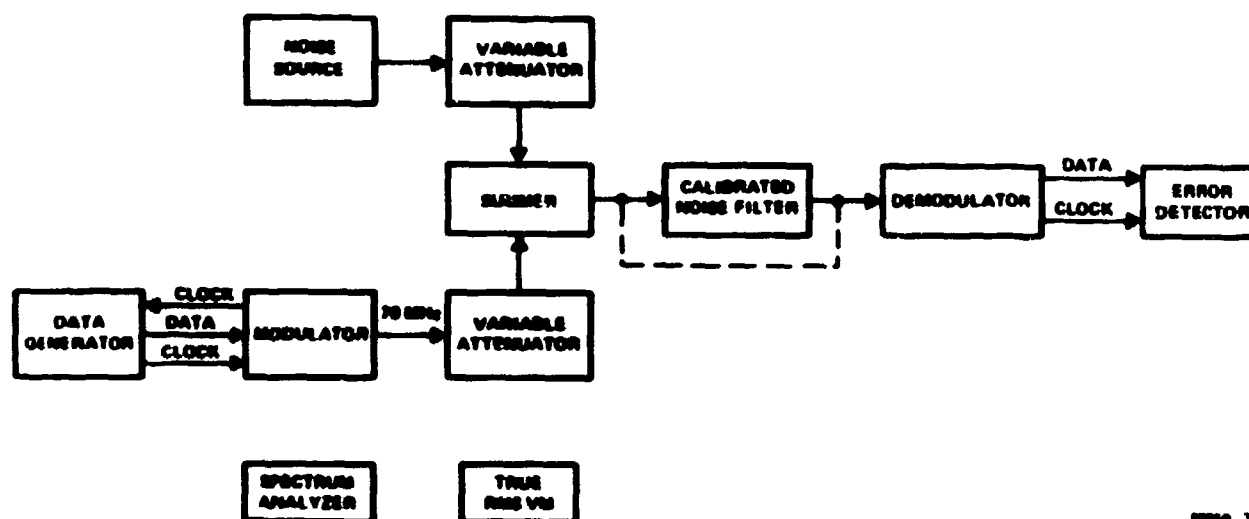
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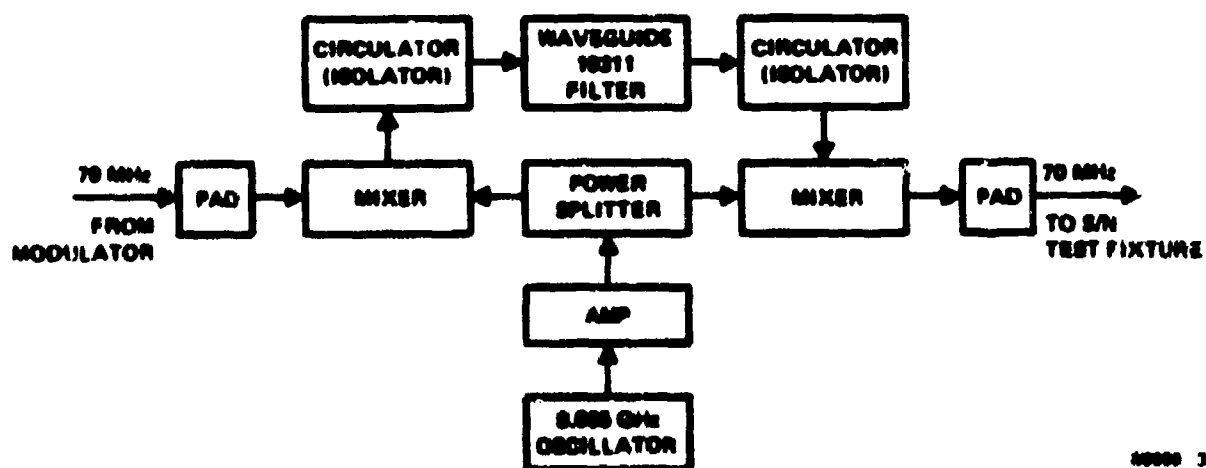Figure C-3. In-Plant Test Configuration

Figure C-4. Up/Downconverter for In-Plant Waveguide Filter Tests

the plotted transmitter spectrum falls on or below the mask, the FCC 19311 requirements will have been met. The test is performed for both 1 B/Hz and 2 B/Hz operation.

4.1.2 E_b/N_o Calibration

The calibration of E_b/N_o is accomplished directly at the demodulator input. The signal attenuator is set at 120 dB and the noise power is measured using a filter with a known noise bandwidth. The noise bandwidth is established by graphical integration techniques. The noise attenuator is then set at 120 dB and the signal power is adjusted to give the same meter reading as the noise power did previously. The noise attenuator is then restored to its original position, establishing a 0 dB SNR in the filter bandwidth. E_b/N_o is then determined by adding a correction factor that is equal to 10 log $\frac{NBW}{BR}$ where NBW is the measured

noise bandwidth of the calibrated filter and BR is the bit rate. The desired E_b/N_o is obtained by adjusting the attenuator setting.

4.1.3   Bit Error Rate Versus E_b/N_o

The objective of this test is to characterize the BER performance of the modem over the range from 10^{-2} to 10^{-9} as a function of E_b/N_o. The test setup is calibrated as in Paragraph 4.1.2. The attenuator is adjusted to provide an E_b/N_o of 10 dB. The error detector is adjusted to provide an error sample of at least 100 events. The indicated error rate is recorded on seven cycle semilog paper. The attenuator is adjusted to provide an E_b/N_o of 11 dB and the indicated error rate is recorded. This process is repeated until an E_b/N_o of 22 dB is reached. The test is performed with the modulator and demodulator back-to-back and also with the up/downconverter and RF filter. Results are obtained for both 2 B/Hz and 1 B/Hz operation.

4.1.4   Acquisition

The objective of this test is to determine the time interval required for the demodulator to acquire synchronization following the

application of IF signal. The design objective is 20 ms at an E_b/N_o corresponding to a $1 \cdot 10^{-7}$ BER with a frequency offset of 20 kHz. A diagram of the test setup is shown in Figure C-5. The 70 MHz IF is offset by replacing the modulator's internal 97.658125 MHz LO with a frequency synthesizer or stabilized oscillator. Varying the frequency of this source will directly vary the center frequency of the modulator output. The IF signal plus noise is gated on with a digitally controlled switch. The switch control signal also triggers an oscilloscope which monitors the error output of the demodulator. The time of transition from a 50 percent error rate to one of $1 \cdot 10^{-7}$ can be observed on the scope and the time interval noted. The test is run with both the 2 B/Hz operation and 1 B/Hz operation.
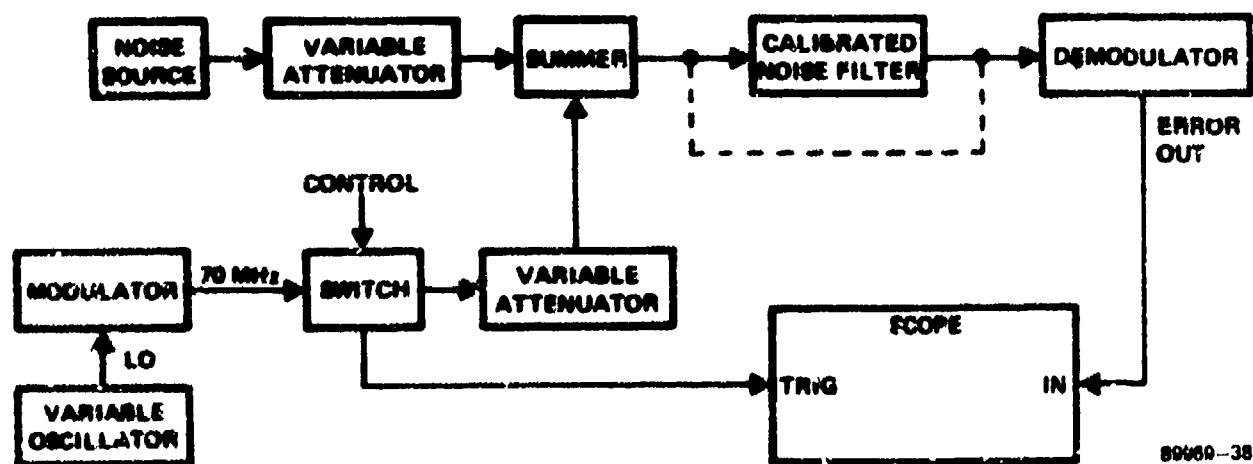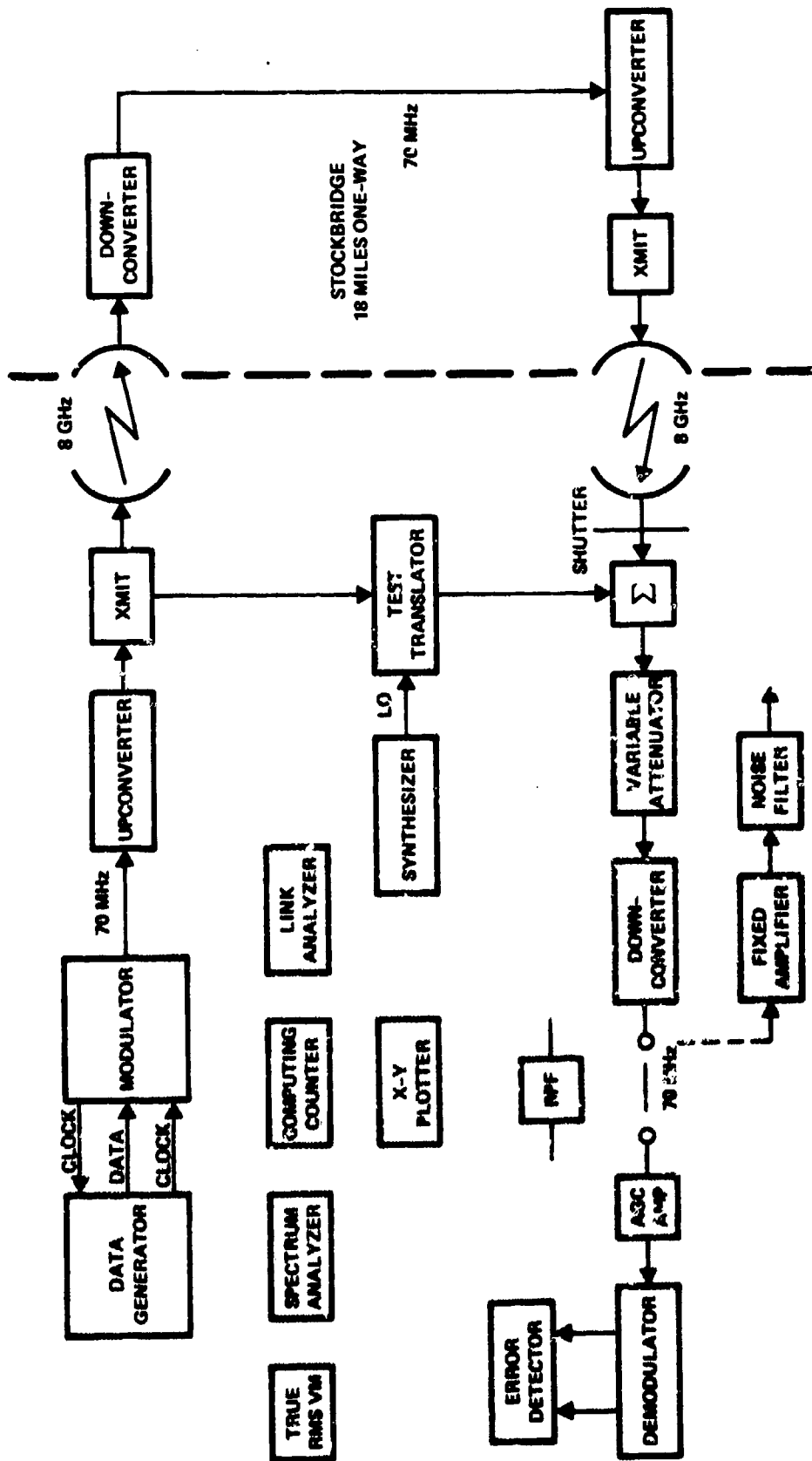

Figure C-5. Acquisition Test Set Configuration

4.2 RADC Tests

The test configuration for the RADC tests is shown in Figure C-6. The overall objective of these tests is to characterize the modem performance when interfaced with the LC8D radio. The link analyzer is used to document the amplitude and delay characteristics of the test configuration.

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Figure C-6. RADC Test Configuration

4.2.1 Spectral Occupancy

The objective of this test is to determine the degree to which the transmitted spectrum conforms to the requirements of FCC 19311. The modulator output is applied to the upconverter and the 8.075 GHz spectrum filtered with the waveguide filter is plotted with the spectrum analyzer and X-Y plotter. Results may be compared with the 70 MHz spectrum to determine the effects of the filter.

4.2.2 E_b/N_o Calibration

The calibration of E_b/N_o is accomplished directly at the demodulator input. A fixed gain amplifier is required outboard to the radio to provide the power level necessary for the HP 431C meter. With the waveguide shutter closed and the simulator configured for loop back at 8 GHz, the downconverter (D/C) noise is read through the calibrated filter with the receive attenuator set at 90 dB. The attenuator is then decreased until the meter reading increases by 3 dB which indicates the SNR in the calibrated filter is 0 dB. As described in Paragraph 4.1.2, E_b/N_o is 0 + K dB at this point, where K is the correction factor for the noise filter. The desired E_b/N_o is obtained by adjusting the attenuator setting.

4.2.3 Bit Error Rate Versus E_b/N_o

The objective of this test is to characterize the BER and the recovered clock jitter performance of the modem as a function of E_b/N_o. Tests are run with the simulator looped at 8 GHz and over the link to Stockbridge and back. The test setup is calibrated as described in Paragraph 4.2.2. The receive attenuator is used to adjust E_b/N_o in 1 dB steps. The BER is recorded at each step to produce a complete 7 cycle graph of performance as a function of E_b/N_o. The computing counter is used to measure recovered clock jitter as appropriate. Tests are run with and without the FCC 19311 waveguide filter and for both 2 B/Hz and 1 B/Hz operation.

5.0   TEST DATA EVALUATION

The test results will be analyzed and provided in the Final Report